



Published on *edacentrum* (<https://project.edacentrum.de>)

[Home](#) > [Projects](#) > [Printer-friendly PDF](#)

# CLEAN: Controlling leakage power in NanoCMOS SoCs



With the advent of nanometric devices, the relevance of leakage power has grown tremendously. All technology roadmaps, as well as the results from advanced semiconductor labs indicate leakage as the real showstopper for the future generations of nanoelectronic circuits if proper counter-measures will not be taken. To be successful, and thus leading to the capability of fabricating chips with sub-65nm technologies, such counter-measures must be rooted in the design domain, as process improvement will not be sufficient to cope with the increased leakage currents in MOSFETs. In other terms, time has come for considering leakage reduction also a design problem, and not only a technology problem.

CLEAN will contribute in a decisive way to the solution of the problem of controlling leakage currents in CMOS designs below 65nm, which is of strategic importance in the ASIC and SoC design landscape. The RandD effort will crystallize around the development of new leakage models for nanometric technologies usable at different levels of abstraction, from device to behavioral, innovative circuit and architectural solutions for efficient leakage management, novel methods and prototype EDA tools for automatic leakage minimization. Such methods and tools will be integrated into commercial EDA frameworks, thus providing comprehensive solutions for power-driven design.

The CLEAN Consortium features the right mix of competence (semiconductor vendors, EDA vendors, research institutes) and the appropriate mobilization of resources to guarantee the successful achievement of all the project objectives. Tight links to on-going European projects targeting advanced silicon technology development (e.g., the NanoCMOS IP and its possible successor, PullNano) will guarantee synergy and convergence of objectives, towards the establishment of design capabilities that will be key for consolidating and growing the European competitiveness in the nanoelectronics business of the future.

---

## Funding initial:

EU FP7 IST-4-026980

## Runtime:

Tue, 01 November 2005 - Fri, 31 October 2008

## Website:

[http://cordis.europa.eu/projects/rcn/80561\\_en.html](http://cordis.europa.eu/projects/rcn/80561_en.html)

## Used Abbreviations

Abbreviation	Meaning
PR	Project Report
SPR	Short Project Report
PN	Project News
FPR	Final Project Report

edacentrum | Schneiderberg 32 | 30167 Hannover | fon: +49 511 762-19699 | email: [info@edacentrum](mailto:info@edacentrum.de) [dot] deup

---

