# Content

# Preface

Currently we are witnessing the transition of microelectronics to the new world of nanoelectronics. This transition together with all its new options, such as "More Moore", "More than Moore" and "Beyond Moore" means completely new challenges concerning the design of future electronic systems. edaForum07 will demonstrate that EDA is a decisive factor to convert these new challenges to fabrication data by which the fabs can be fed in order to turn silicon-wafers into valuable chips.

„More Moore" focuses on further scaling leading to higher speed and less power consumption enabling cheaper products. EDA has to master the exponentially increasing complexity and is faced not only with the increasing hardware design gap, but with an even larger software design gap. Therefore, edaForum discusses this year "how hardware and software can team up in a better way?" "More than Moore" allows functional diversification and means that new devices like RF, sensors, and actuators in even new technologies have to be developed and integrated, which do not necessarily follow the scaling of Moore's Law. Experts will share their view on the question "mixed signal integration: all done?"

edaForum taking place for the sixth time will stick to its successful and unique concept of combining technical and business-oriented topics. The combination of both fields is the special attribute that makes the edaForum so unique. It will be decisive for further developments in the field of nanoelectronics, if we are successful in gaining a foothold in new markets like health and medical applications. We therefore have invited experts to show how „microelectronics meets medicine." Last but not least our invited speakers will discuss with you the semiconductor industry consolidation. Many IDMs have been forced to remodel their businesses in order to become "fablite" or even fabless. We are curious about their and your answers to our question "how many will survive?"

Join us and seize the opportunity to discuss your questions with our invited experts concerning the challenges and possibilities of EDA. The edacentrum cordially invites you to this year's edaForum and I am really looking forward to welcoming you all in Munich. I hope to see you all there!

**Wolfgang Rosenstiel**
Chairman edacentrum

**Hermann Eul, Infineon**

# Beyond IC Design – Challenges for the Next Generation of EDA Software



Internet and Mobile Communication represent the revolution in communication technology in the past two decades. Only 17 years after release of the GSM standard more than 2.5 billion mobile phone users worldwide are registered in 2007. Market observers expect a sales volume of more than 1 billion handset devices in 2007.

In May 2007 Infineon has released the 2nd generation of an Ultra Low Cost mobile phone system platform. The ULC platform enjoys technological leadership since Infineon was first in the successful integration of mobile phone baseband IC with the RF transceiver on a single SoC in standard CMOS technology.

During the development of this platform we faced the challenge that the available EDA tools do not sufficiently support the development of such complex systems. We derived 3 major areas in which we expect the EDA industry to contribute with innovative solutions in the near future. Especially the larger EDA vendors are required to move here more quickly as they provide key components of the EDA design system infrastructure used by the semiconductor industry.

First importance has the seamless integration of system development, firmware development and circuit design. It is of utmost importance to have these three development processes synchronized from the early architectural exploration until final system verification and validation.

Any mismatch of modeling and simulation increases the risk of system failure and cause difficulties in the qualification of the circuits. In this area we would like to see more engagement by the EDA/IP industry towards the development and adoption of open standards ensuring a reliable system design flow over the complete development cycle.

Secondly the significant progress in RF-CMOS implementation allows an integration of highly complex digital components with analogue RF-blocks on the same silicon die. Today the design teams experience the absence of integrated development and verification solutions. Insufficient pre-silicon verification results in costly re-design cycles. Here the EDA industry is asked to integrate their respective functionality to more complete environments.



The third area for improvement is the growing interdependency between circuit and package design. A prominent example is the new Wafer-Level-Ball Grid (WLB) packaging technology which is the next step towards the BoM reduction. Today the EDA industry does not provide sufficient support for the concurrent and integrated design of both circuit and package forcing the semiconductor industry to compensate this with additional efforts and internal tools.

**Hermann Eul**
Member of the Management Board
Executive Vice President
Head of Communication Business Group
Infineon Technologies AG

Professor Hermann Eul studied electrical engineering and has a doctorate and professorate in engineering.

Until 1999 Professor Eul was General Manager of the Digital TeleCom and Data Com ICs operations at Siemens.

When Infineon was formed, he took over the Wireless Baseband and Systems Business Group as Vice President and General Manager. From 2001 to 2002 he was responsible for Security & Chip Card ICs operations as Chief Executive Officer.

In 2003 he was appointed as full Professor and Head of Faculty Chair for RF-Technology and Radio-Systems at the Hanover University. In 2004 he returned to Infineon where he first managed the Wireline Communications business group as Senior Vice President and General Manager and then, following the reorganization, he became the Group Vice President and General Manager of the Communication Solutions business group.

Professor Eul became a member of the Infineon Management Board in July 2005. He is responsible for the Communication Solutions business group.

# "WOULDN'T IT BE NICE"
# Microelectronics Meets Medicine

**Session Keynote:**

**Bernhard Wolf, Technical University of Munich**

## Microelectronics Meets Medicine ($m^3$): Electronic Systems for Diagnosis and Therapy



A comparison of practical achievements of microelectronics in the last 30 years to those of biotechnology proves a by far much higher contribution of microelectronic products to the emancipation of the individual man and the economics, than expected by the most daring molecular biological visions.

From the economic point of view there are to note the large value creation chain, high quality and number of jobs as well as the high innovation potential.

No modification in our life was so completely accomplished like this one by technology such as telephone, fax, radio, TV, GPS, and last but not least the PC world, apart from the numerous microprocessor systems hidden in consumer goods and traffic systems.

The demographic composition of today's population and the cost development in health service suggest to turn intensively towards the abilities of microelectronic techniques and systems in health service and to use them consequently. The cultural contribution of microelectronics can not be overlooked and, as indicated in the past, even high-priced systems became inexpensive, indeed cheap, consumer goods of daily life allowing access and use of these high-tech products also for not so wealthy social strata. Their advantage in use for health services is not limited to aged of handicapped people. The same systems serving to locate schoolchildren at non-open and dangerous school ways, for training control of sportsmen, health control of high-risk patients can, of course, also be used later for elder people, to give them more autonomy, while simultaneously minimizing risks and increasing quality.

Some examples will be illustrated in this presentation.

**Bernhard Wolf**
Head of the Heinz-Nixdorf Chair for Medical Electronics
Director of Institute of Medical Engineering (IMETUM)
Technical University of Munich

Bernhard Wolf is Professor, head of the Heinz-Nixdorf Chair for Medical Electronics and Director of Institute of Medical Engineering (IMETUM) Technical University of Munich, Germany. His research interests include the development of bioelectronic systems for biomedical diagnostics and therapy.

**Thursday, Dec. 6, 2007**
**2:20 pm — 3:05 pm**
**Salon C/D**

**Bernd Flick, Technical University of Berlin**

# A Microelectronic Telemetrical Measurement System for Intracranial Pressure and Temperature



Microsystem technologies (MST) have become the basis of a new industry. The advantages of MST compared to other technologies provide opportunities for application in implantable biomedical devices. This presentation shows how a fully implantable stand-by device for measuring intracorporal pressure and temperature under normal conditions can be implemented, consisting of a sensor element combined with a transcutaneous telemetric interface without the use of energy storing components like batteries. The measurement of intracranial pressure (ICP) is very uncomfortable for the patient today. For more comfort and mobility, a portable measurement unit for parameter calculations is proposed. It consists of an implant in the head with a pressure sensor, a second one outside the head and a portable data recorder including a display. The aim of the subject is to calculate the compliance and resorption and to measure ICP under daily conditions.

One further point of interest is automatic event recognition in order to capture special signal components in an emergency situation. Therefore, signal processing and waveform analysis are exigent, first to observe the measured signal in realtime on a portable unit, and second to process the data offline on a stationary unit.

**Bernd Flick**
Institute for electronics and medical signal processing
Technical University of Berlin

Bernd Flick was born in Germany in November 1965. He received the Dipl.-Ing. Telecommunication (FH) with high honors from Fachhochschule Deutsche Bundespost Telekom, Berlin, in 1990. He received the Dipl.-Ing. degree in electrical engineering in 1994 and the Dr.-Ing. degree in electronics in 1999, both from the Technical University of Berlin.

He spent six years as a full time electronics research and design engineer for medical microelectronics implantations at the Sican F&E GmbH in Hannover while in Technical University and after. After changing to the corporate research center of Robert Bosch GmbH, he developed another five years multimedia systems for medical and automotive applications.

# "WOULDN'T IT BE NICE"
# Microelectronics Meets Medicine



**Thomas Schweizer, Aipermon**

## Innovations in Telemedicine

Demographical changes in the aging structure and changes in the way of living regarding malnutrition and lack of exercise lead to an increase of chronic diseases. Additionally the pressure for cost savings in the health care system increases. Thus, new medical care concepts in the area of telemonitoring arise.

In the first part, the presentation gives an overview of telemonitoring solutions and shows technical requirements concerning low power concepts, interfaces for medical devices, zero-button handling, data security and data reliability. The second part covers a new activity sensor concept (AiperMotion) based on a low g 3-dimensional acceleration sensor. The AiperMotion captures all activity data of a person for 7 days by a continuous measurement and storage and provides an opportunity for telemetrically transmission. Finally the medical areas of application will be described and how a measurement device can motivate to more exercise.

**Thomas Schweizer**
General Manager
Aipermon GmbH & Co. KG

Dr. Thomas Schweizer is general manager of Aipermon GmbH & Co. KG and is one of the founding members of the company.

Dr. Schweizer started his professional career at Robert Bosch GmbH. In 1996 Dr. Schweizer moved to Siemens HL in the field of chip cards and security ICs. Until 1999 he was head of the Product Analysis and Product Development departments. From 2000 he was head of development for Chip card and Security ICs (Infineon Technologies AG) and held worldwide responsibility for innovation, specification, technology and product development, as well as system engineering. In 2002 he set up and managed "Innovation and Concepts" in the Secure Mobile Solutions business division within Infineon. From 2004, Dr. Schweizer oversaw the implementation of the telemonitoring technology in the Emerging Business division at Infineon.

Dr. Schweizer helds a degree in physics from the Albert-Ludwigs University in Freiburg.

**Thursday, Dec. 6, 2007**
**4:05 pm — 4:35 pm**
**Salon C/D**

**Following its triumphal procession, microelectronics is close to a next wave of useful applications. Medical equipment in its widest sense is a very promising candidate.**



**Matthias Schönermark, Hannover Medical School**

# Economical and Strategic Aspects of Medical Innovation Markets

Clinical medicine and the medical industry behind it have been showing dramatically increasing innovation and complexity dynamics, which resemble the history of microelectronics in the last 40 years. However, a Moore's law has not been formulated yet. As information is the glue in the medical value chain, it is compelling that the evolutionary power of microelectronics has an enormous impact on the medicine of the future. The lecture will discuss the currently detectable forces of the microelectronics science and industry which have an observable impact on clinical medicine and will speculate on the most promising and exciting fields where both disciplines might interact in the future.

**Matthias Schönermark**
Professor of Management, Hannover Medical School
Managing Director, Center for Biomedical Technology and Innovation (BiomeTI)
CEO Schönermark.Kielhorn+Collegen

Born in Essen in 1964, Professor Matthias Schönermark graduated magna cum laude in Theoretical Medicine at the University of Heidelberg in 1991, followed by a post-doc scholarship at the Institute of Immunology at the University of Heidelberg, his qualification exam of Otolaryngology/Head and Neck Surgery, his habilitation with a Ph. D. thesis in Molecular Oncology in 1998 and his appointment to a professorship of management at the Hannover Medical School in 2000. From 2001 – 2005 he was Vice President of the Hannover School of Health Management which he initiated and founded.

He is lecturer for "Strategic Management of Health Care Institutions' and "Technology and Innovations Management" at the Hannover Medical School, Krannert School of Business Administration, Purdue University/USA, Ajman University for Science and Technology, Ajman/UAE, and Tias Business School, Tilburg/NL. He is a permanent consultant to numerous CEOs of international health insurance and provider organizations, as well as of medtech and pharma companies on strategic management, innovation management and change management issues.

**Thursday, Dec. 6, 2007**
**4:35 pm — 5:05 pm**
**Salon C/D**

# "STILL HAVEN'T FOUND WHAT I'M LOOKING FOR"
# Mixed Signal Integration: All done?

**Session Keynote:**

**Georges Gielen, Katholiek Universiteit Leuven**

## Analog Design Automation: Dream or Reality?



CMOS technology scaling into the nanometer era has enabled the integration of entire systems, many of which containing analog interface circuits and/or RF radios on the same die. To manage the increasing complexity of these integrated systems, electronic design automation tools are indispensable to improve design efficiency and to limit design risk. This presentation gives an overview of the progress in analog EDA that has been accomplished over the past two decades of intensive academic research and commercial startup activities. Advanced simulation techniques, behavioral modeling, circuit optimization and layout synthesis are all a reality today. Still, not every analog designer in industry has fully embraced these new tools in his/her daily practice. With nanometer technologies bringing even more challenges of increased variability and aggravating signal integrity conditions that require proper modeling and analysis tools, how much longer can analog designers continue the old-fashioned way and outdate themselves?

**Georges Gielen**
ESAT-MICAS,
Department of Electrical Engineering
Katholiek Universiteit Leuven

Georges G.E. Gielen is Full Professor in Electrical Engineering at the Katholieke Universiteit Leuven. His research interests are in the design of analog and mixed-signal integrated circuits, and especially in analog and mixed-signal CAD tools and design automation (modeling, simulation and symbolic analysis, analog synthesis, analog layout generation, analog and mixed-signal testing). He has authored or coauthored five books and more than 300 papers in edited books, international journals and conference proceedings.

His work has also resulted in several spin-off companies. He served as General Chair of the DATE conference in 2006 and of the ICCAD conference in 2007. He is a Fellow of the IEEE and served as President of the IEEE Circuits and Systems (CAS) Society in 2005. He was elected DATE Fellow in 2007, and received the IEEE Computer Society Outstanding Contribution Award and the IEEE Circuits and Systems Society Meritorious Service Award in 2007.

**Thursday, Dec. 6, 2007**
**2:20 pm – 3:05 pm**
**Salon A/B**

**Werner Geppert, Infineon**

# RF & MS Integration Challenges in Single Chips for Mobile Phone Applications



Starting with the 130 nm node, subtle physical effects lead to unexpected re-spins and drastically increased efforts in the device modeling and circuit design departments. Architectural changes to digitize analog functionality have been identified as one viable option to cope with these effects.

With the RF move from bipolar to CMOS and the following single chip integration new challenges were introduced such as 1/f noise and RF/digital interference. The later ones being extremely complex as the effects involve the die itself, the redistribution layer, more than 200 balls to be connected to the printed circuit board and the board itself.

Main driver of Moore's Law is to take advantage of higher complexity at lower pricing. Remaining still true for mostly digital products, products with a high content of Analog or RF circuits do not scale anymore in the same amount as the digital circuit portions, so that the cost advantage is decreasing. Even worse, moving functionality to the next node the die size might even become larger without the introduction of complete different architectures. In addition, the integration of functions like power management units on the same die needs special devices to deal with the high voltage requirements. Therefore, the economical benefit of brute force node to node migration has to be questioned.

**Werner Geppert**
Head Design Methodology
Communication Solutions
Base Technologies and Services
Infineon Technologies AG

Werner Geppert was born in Essen, Germany, 1964. He received his Dipl.-Ing. and Dr.-Ing. degrees in electrical engineering from Ruhr-University Bochum, Germany in 1991 and 1996, respectively. 1996 he joined the RF division of SIEMENS Semiconductors as RF circuit designer for cordless products. In 1998 he became responsible for RF design technology. In 1999 he took over the position as design center manager of the SIEMENS Microelectronics RF group in Princeton, NJ. Between 2002 and 2006 he held various engineering management positions within Infineon Germany, with main responsibility being the head of the RF & MS design methodology group of the communications division (COM). Since early 2006 he is the head of overall design methodology at COM which includes global teams for System-, RF/MS- as well as digital design methodology and global support teams as interface to all R&D projects.

**Thursday, Dec. 6, 2007**
**3:35 pm — 4:05 pm**
**Salon A/B**

# "STILL HAVEN'T FOUND WHAT I'M LOOKING FOR"
# Mixed Signal Integration: All done?

**Oscar Buset, Kimotion**

## Analog Design Tools for Nanometer Processes



The need for analog design and verification software is on the rise. Mixing analog and digital circuits on single-chip SOCs can strain or break old tools and methodologies in a number of ways, whether it be trying to match digital design turnaround times, ensuring first-time silicon success, or dealing with statistical data in nanometer process technologies.

Traditional analog design methodologies face significant challenges with advancing process geometries. An important issue amongst these is the overdesign incurred when designing to classic worst-case corners - corners traditionally derived for digital circuits, but used also to ensure the robustness of analog cells. The best current alternative, monte-carlo simulations, can be prohibitively expensive in terms of run time, given the number of simulations necessary to confidently predict the distribution of the performances of a design.

This talk will focus on how new software and flows can help analog design teams cope with statistical process technologies.

**Oscar Buset**
President
Kimotion Technologies

Oscar Buset is president of Kimotion Technologies since its founding in 2003. Prior to Kimotion, Dr. Buset founded Snaketech and served as vice president responsible for place and route products until Snaketech's acquisition by Simplex Solutions in 2000 (since acquired by Cadence). He holds a PhD. from EPFL (Swiss Federal Institute of Technology) and M.Sc. (Electrical Engineering) and B.Math. (Computer Science) degrees from the University of Waterloo, Canada. From 1988 to 1990, Dr. Buset worked in the CAD department of Bell-Northern Research (now Nortel), focusing on analog simulation. He has several patents in the field of physical design.

**Thursday, Dec. 6, 2007**
**4:05 pm — 4:35 pm**
**Salon A/B**

**Wolfgang Fichtner, Synopsys**

# Breaking Down the Manufacturing Design Firewall - DFM Flows are Becoming Reality



Since the early days of wafer processing the separation of design and fabrication has worked impressively well for many generations of technology. At 130nm and below, however, many physical effects have begun to strain this ability, leading to a gap between design and silicon performance. If this gap becomes too large, it becomes impossible to manufacture a design at high yield due to systematic and random factors. Mixed signal and analog designs in smaller geometries put additional DFM requirements.

To reduce the design-manufacturing gap, three options exist: 1. to improve the models; 2. to modify the manufacturing process; and 3. to improve both. The first solution (DFM in the traditional sense) encompasses additional tools and methodologies that are introduced in the design flow and the post processing of the GDSII layout database prior to mask manufacturing. The second solution focuses on tools and methodologies introduced in manufacturing to mitigate factors influencing parametric yield (called "Manufacturing for Design" or MFD).

This talk will review the current status of DFM and MFD efforts in the semiconductor and EDA industry and will especially discuss the DFM requirements for analog and mixed signal designs.

**Wolfgang Fichtner**
Senior Vice President a.General Manager
Silicon Engineering Group
Synopsys, Inc.

Wolfgang Fichtner received the M.S. degree in physics and the Ph.D. degree in electrical engineering from the Technical University of Vienna, Austria, in 1974 and 1978, respectively. From 1979 through 1985, he worked at AT&T Bell Laboratories, Murray Hill, NJ. He was Professor and Head of the Integrated Systems Laboratory at the Swiss Federal Institute of Technology (ETH) from 1985 to 2004.

In 1993, he founded ISE Integrated Systems Engineering AG, a company in the field of TCAD. In November 2004, he joined Synopsys Inc, Mountain View, CA, as Vice President and General Manager of the TCAD Business Unit. He is currently Senior Vice President and General Manager of the Silicon Engineering Group at Synopsys. In 2000, he received the IEEE Andrew S. Grove Field Award for his contributions to TCAD. In the areas of integrated circuit design, Technology CAD and solid state physics, he has published more than 450 papers.

**Thursday, Dec. 6, 2007**
**4:35 pm — 5:05 pm**
**Salon A/B**

# "I WILL SURVIVE"
# Semiconductor Industry Consolidation

**Session Keynote:**

**G. Dan Hutcheson, VLSI Research**

## Semiconductor Industry Consolidation: Who will survive?



The change from micro to nano-manufacturing has created problems and opportunities throughout the semiconductor manufacturing food chain, from design to test and packaging. The challenge of nano-manufacturing has driven the companies to undertake an increasing number of corporate re-structuring activities, which not only include mergers and acquisitions, but spin-offs as well.

The presentation concentrates on the opportunities that nano-manufacturing has created for chip designers, EDA and manufacturing. It also addresses several critical questions: Is the current business environment increasing the industry consolidation? Or is the design and manufacturing specialization a more prevalent trend, and why? What is the role of foundries, and can chipmakers still differentiate through manufacturing? Is there an opportunity for designers to influence the current trends? The companies that are able to master these challenges and turn them into strengths that can be exploited in today's market place are the future winners.

This keynote presentation is based on VLSI Research's databases and analysis to provide viewpoint to these critical trends.

**G. Dan Hutcheson**
CEO
VLSI Research Inc

Dan Hutcheson is CEO of VLSI Research Inc. He is a recognized authority and well-known visionary for the semiconductor industry whose career experience spans more than twenty years. Today Hutcheson spends the majority of his time advising companies in strategic and tactical marketing, business management, and manufacturing trends, productivity, and strategy. During his career, Hutcheson has authored numerous publications, developed many industry models, and researched most aspects of the semiconductor industry. Hutcheson is probably best known for being the first to forecast an industry recession and for having developed the industry's first cost-of-ownership model in the early eighties. Hutcheson holds a master's degree in Economics from San Jose State and has completed additional engineering coursework from UC Berkeley.

**Friday, Dec. 7, 2007**
**9:00 am — 9:40 am**
**Salon C/D**

**Nowadays the system of global, diverse and complex businesses is a risky environment where you legitimately ask for survivors.**

**Craig Johnson, Cadence**

# Solutions for Enterprise Product Development



We are witnessing an evolutionary change in the electronics industry. Innovation in the electronics industry was traditionally driven by IT. It is now more and more driven by consumer behavior, which is impacting the dynamics and economics of the semiconductor value chain. Value to the end user is being delivered through content and applications, while the underlying hardware experiences huge cost and time-to-market pressures. As systems market segment share consolidates to fewer players, companies are placing larger bets on their semiconductor suppliers. This may ultimately lead to accelerated consolidation within the semiconductor industry. With huge investments dependent upon flawless product delivery, the systems and semiconductor companies need design automation capabilities which address both their productivity and execution requirements. This talk will describe how EDA and taking Cadence as an example is evolving to meet these challenges which will enable customers to enjoy increased business success.

**Craig Johnson**
Corporate Vice President, Marketing and Strategy
Cadence Design Systems, Inc.

Craig Johnson is Corporate Vice President, Marketing and Strategy at Cadence, reporting to Michael J. Fister, President and CEO. In this role, Johnson is responsible for driving the company's strategic agenda, the definition of innovative products and solutions as well as for related go-to-market and business strategies.

Johnson joined Cadence in 2004 as Vice President, Strategy and Planning before he took over the Marketing organization early this year. Prior to Cadence, Johnson spent 11 years at Intel in a variety of positions. His last position there was as Director of Strategic Marketing in Intel's Enterprise Platforms Group.

Johnson holds a B.S. degree in electrical and computer engineering, as well as a Masters of Business Administration, both from Brigham Young University.

**Friday, Dec. 7, 2007**
**9:40 am — 10:05 am**
**Salon C/D**

# "I WILL SURVIVE"
# Semiconductor Industry Consolidation



**Thilo von Selchow, ZMD**

## Transformation of an East German Technology Portfolio into a Medium-Sized Global "Fabless Company" in the Analog Mixed Signal Segment

After the privatization of the 46 years old company ZMD in 1999 first revenues were generated with a lot of "rainmaking skills" from rich existing technology portfolio.

However, it was not possible to find enough funding and investors to fund all the existing business models which still existed under the ZMD umbrella.

Therefore, it was necessary to focus ZMD onto the small but profitable field of being a fabless company in analog mixed signal for enabling sensors.

Our Philosophy is the simple strategy "to capture" several application markets, which are "under the radar screen" of interest for large companies. ZMD is now very successful and fast growing.

Confirmation for this business model is found in the fact that small companies have continued to be the basis of many innovations, fast and flexible solutions in addition to the large firms.

This variety of some large and many small companies adds to each other and has been in the past and will be also in the future the basis for a healthy, innovative, strong German economy.

**Thilo von Selchow**
CEO and President
ZMD AG

Thilo von Selchow is CEO and President of ZMD AG since eight years. Also he is a cofounder of "Silicon Saxony e.V.," Europe's largest microelectronics cluster and has been the association's President for the first six years.

He studied mechanical engineering and business economics at the University of Munich from 1983 to 1989. He holds a degree in Economics.

Between 1990 and 1991, he was Investment Manager at the BfM AG Munich. In 1991 he attended the Harvard Summer School in Boston. Following this, he joined the Heikamp & Thumann Group, where he served in several management positions between 1991 and 1999. In 1997 he became the Managing Director of the Heitkamp and Thumann Group.

**Friday, Dec. 7, 2007**
**10:35 am — 11:00 am**
**Salon C/D**

**Nowadays the system of global, diverse and complex businesses is a risky environment where you legitimately ask for survivors.**

**Josef Winnerl, Infineon**

# Smart Technology Access - How to Position in the Semiconductor Value Chain



In the recent years the semiconductor industry landscape changed significantly. Cost became a real issue – developing advanced technologies and building manufacturing lines for such technologies are no longer affordable for the majority of semiconductor suppliers. Only a few individual companies try to maintain their traditional IDM model, while the majority of successful companies is forming alliances. Life is also getting tougher for fabless and foundry companies in their traditional domains of the value chain. Foundries are no longer pure contract manufacturers; they try to differentiate through design enablement and IP offering - a traditional IDM domain. And a fabless company without an insight into technology has a hard time to efficiently bring products to 65nm and beyond.

The presentation will describe the key trends and success factors for successful companies in our business.

**Josef Winnerl**
Vice President
Technology Development
Communications Business Group
Infineon Technologies AG

Josef Winnerl is Vice President for Technology Development in Infineon's Communication Business Group. He is responsible for the development of CMOS platform technologies including GDS2 mask flow, modeling and design enablement. Before joining Infineon he has been with Siemens Corporate R&D Center and Semiconductor Group of Siemens serving in different management positions in CMOS technology and embedded Flash process and design development. He received his Diploma in 1983 and his PhD in 1984, both in Electrical Engineering from the Technical University of Munich.

**Friday, Dec. 7, 2007**
**11:00 am — 11:25 am**
**Salon C/D**

# "LET'S STICK TOGETHER" Hardware and Software Team up!

**Session Keynote:**

**Mikko Terho, Nokia**

## Are EDA tools for Systems Architecture, ASIC Design or Agile Software Development



Nokia has traditionally used EDA tools for ASIC development on the RTL level. However currently more and more responsibility of the SoC design of traditional mobile phones is taken up by the semiconductor vendors. Handset vendors focus is nowadays on system design and software developments. How can EDA tools be used in these tasks or are they becoming irrelevant?

Nokia has used model based tools and tools using high level abstract languages to get early visibility to design choices in systems architecture and power consumption. The presentation will describe experiences in the use of Bluespec modeling to make software and hardware tradeoffs.

Nokia Software Platforms (S60 and Linux Internet Tablets) are moving to use agile software development methods and daily build lifecycle. There has been a demand to build a "Tasking Accurate and Binary Compatible" virtual platform of the core product. Ideas and the direction how to go forward in these activities will be presented.

Also,a "Virtual Platform" will be described, which could be used to improve in embedded software maintenance.

**Mikko Terho**
Vice President and Nokia Fellow
Nokia Corporation

Mikko Terho heads Nokia's Intelligent Connectivity Group which focuses on the development of the innovations and prototypes for pervasive communication devices with novel internet services. He also advices as Nokia fellow other Nokia R&D Groups in the area of system design, software architecture and component selection. Terho joined Nokia in 1983 and has served since in various research and development and managerial positions within the company. Prior to the current assignment Terho was head of the Strategic Architecture group at Nokia Technology Platforms. He has been responsible for development of early WCDMA phones and the development for Nokia communicators. He is also a founding Director of Wireless Application Protocol (WAP) Forum Ltd and Director of Symbian Ltd.

Terho has a M.Sc. from the Tampere University of Technology. He has over 40 granted patents in the area of Wireless Communication and Mobile Internet.

**Friday, Dec. 7, 2007**
**9:00 am — 9:40 am**
**Salon A/B**

**Stefan Koerner, IBM**

# Virtual Power on in IBM

IBM's eServer design incorporates besides new microprocessors (power and mainframe architecture) a increasingly amount of firmware to realize virtualization functions, achieve energy savings and reliability features. The time to market and the field quality strongly depend on the quality of that firmware. The talk will explain IBM's "Virtual Power On Concept" which is in use at IBM to verify all server designs. It will cover aspects of software engineering as well as hardware firmware coverification using emulation and acceleration technologies. Finally it will address the required changes in project management that became necessary and show some result data of the last projects.



**Stefan Koerner**
Senior Technical Staff Member
IBM Entwicklung GmbH

Stefan Koerner is a Senior Technical Staff Member at the IBM eServer Hardware Development Group in the Boeblingen laboratories. He joined IBM at Boeblingen in 1981 after receiving a M.S. degree in electrical engineering from the Technical University of Furtwangen. He has held a number of positions in logic design, firmware development and verification. Mr. Koerner holds 3 patents and gives lectures on design of digital systems at the University of Coeducation in Stuttgart.

**Friday, Dec. 7, 2007**
**9:40 am — 10:05 am**
**Salon A/B**

# "LET'S STICK TOGETHER" Hardware and Software Team up!



**Hans-Christian Reuss, FKFS**

## Challenges in Testing Electronic Control Units for the Automobile

Automatic test execution has become the state-of-the-art way of testing ECUs over the last years. It eliminates error-prone manual testing, allows regression testing, is cheaper in the long run and faster than manual testing. Different manufacturers offer a wide choice of soft- and hardware to aid the development engineer in his automatic testing activities.

A totally different question is the design of the test-cases themselves. Today there's no way to automatically generate test-cases for automotive ECUs. The main reason is that automatic generation of test-cases would require some sort of formal description of the object that needs testing. There's no such formal description of ECUs in the automotive domain or even for any sort of embedded system. One goal of this contribution is to introduce a process that includes a formal description of automotive ECUs, a connected strategy to automatically obtain the resulting test-cases and a way to access those test-cases through different test systems. In addition an overview about the challenges of the development of automotive electronics in general will be given and the question how to handle the increasing complexity of automotive electronic systems will be discussed.

**Hans-Christian Reuss**
Chair of Automotive Mechatronics
Research Institute of Automotive Engineering and Vehicle Engines Stuttgart (FKFS)

Hans-Christian Reuss received the Dipl.-Ing. and the Ph.D. degrees in electrical engineering from the Technical University of Berlin, Germany, in 1984 and 1989, respectively. In 1989 Dr. Reuss joined the PHILIPS Semiconductors Application Laboratory in Hamburg. In 1993 Dr. Reuss became professor at Dresden University of Technology. In 2001 he was involved in the establishment of the DaimlerChrysler Competence Center of Electrical and Electronic Architecture and in 2002 he established the Institute of Automotive Mechatronics GmbH Dresden. In 2004 Prof. Reuss took over the chair of Automotive Mechatronics at the Institute of Internal Combustion Engines and Automotive Engineering (IVK) and became a member of the management board of the Research Institute of Automotive Engineering and Vehicle Engines Stuttgart (FKFS).

**Friday, Dec. 7, 2007**
**10:35 am — 11:00 am**
**Salon A/B**

**Jean-Marie Saint-Paul, Mentor Graphics**

# Why should Hardware Designers have a Drink with Software Teams?



The successful development of embedded systems requires the continuous integration of hardware and firmware throughout all stages of the project. While today a lot of Hardware/Software integration issues are only discovered on the physical prototype with the pressure put on project's schedule solutions are needed to make sure software is verified at the same time as hardware.

Transaction Level hardware/firmware simulation aids in making a first functional validation of the firmware while helping to take crucial decisions on the architecture of the hardware. After this first system validation more detailed simulation will be necessary to confirm that the memory subsystem can support the reset and boot-up process. Firmware must be executed against a Register Transfer Level hardware description to verify successful boot-up for example.

As an orthogonal approach to functional verification, software driven tests can expose bus interface and timing errors that classical HDL test benches may miss. As a supplement to manually developed tests, verification teams can adopt big chunks of code from the firmware team. Boot code, hardware diagnostics and the RTOS hardware adaptation layer or board support package are highly relevant to functional verification of the hardware design.

**Jean-Marie Saint-Paul**
European Manager SoC Solutions
Mentor Graphics

Jean-Marie Saint-Paul is a European-wide specialist for next-generation system level solutions at Mentor Graphics. His responsibilities include supporting key customers with leading-edge applications to improve productivity and quality in today's challenging economic and technological environment. He brings more than 10 years of experience in HW/SW co-design and system-level design practices to his role at Mentor Graphics. Saint-Paul started in the electronic industry at SAGEM. He then held management positions in EDA at Innoveda and Summit Design, where he served as a European Technical Manager for system-level design solutions. Saint-Paul has an engineering degree in electronic engineering from ESIEE Paris and a Master of Electronic

**Friday, Dec. 7, 2007**
**11:00 am — 11:25 am**
**Salon A/B**

# Metrics and Tools for Improving Chip Design Productivity

Production productivity and yield were key performance indicators in the semiconductor industry for many years. With today's drastically increased complexity of chip designs, ongoing shrinkage of market entry windows as well as product life cycles due to intensified global competition and the irresistible expansion of the fabless model another kind of productivity becomes the dominating factor: productivity of chip design. That includes the amount of resources needed to do a specific design project as well as the duration of that project.

Rising complexities, limitations on available and manageable team sizes and cost issues result in an indispensable demand for drastically enhancing chip design productivity. Another problem is that the productivity of the circuit developers can not be indicated exactly enough. Knowledge of productivity is imperative to increase the ability to plan development projects.

The company presentations of edaForum07 aim at providing chip designers and project managers of chip design projects with means to measure and to improve their chip design productivity. In a tutorial Martin Radetzki will give an introduction to metrics for measuring productivity, to state-of-the-art solutions in the industry completed as well as to some ongoing research in this field. Following that introduction leading EDA vendors will discuss and present available solutions for measuring and improving your productivity in a panel discussion and an exhibition.

Participating companies:

cadence™

chipvision

concept engineering

MunEDA

OneSpin SOLUTIONS

SYNOPSYS®



**09:00 am — 09:40 am**
Tutorial
**"Metrics for productivity and how to use them?"**
Martin Radetzki, University of Stuttgart

To achieve higher design productivity is an important motivation for investments in EDA tools. EDA users and EDA suppliers would benefit from quantitative productivity measurement as an enabler to optimize the allocation of their investments. However, the non-uniform and immaterial nature of the produced goods, "electronic designs", complicates the definition of a productivity metrics. This presentation gives an overview of the fundamental techniques used in state-of-the-art productivity measurement approaches and points out potential for improvement. We review the current R&D activities in this field and point out the need for cooperation between EDA users and suppliers to facilitate more detailed and meaningful metrics.

**09:40 am — 10:30 am**
Panel
**"Metrics and Tools for Improving Chip Design Productivity"**
Moderator: Jürgen Haase, edacentrum

The panel will discuss metrics and tools which are already available to the designers in order to support their productivity.

**10:30 am — 12:00 pm**
**Exhibition**

The Exhibition complements the tutorial and the panel with individual presentations and demonstrations of the participating EDA vendors:

Cadence Design Systems GmbH
ChipVision Design Systems AG
Concept Engineering GmbH
MunEDA GmbH
OneSpin Solutions GmbH
Synopsys GmbH

**12:00 pm – 1:00 pm**
**Lunch**

All participants are invited to a sponsored lunch.

**Thursday, Dec. 6, 2007**
**9:00 am — 1:00 pm**
**Salon A/B**

# Location

Munich, city of art, culture and tradition, beer gardens is one of the world´s most popular destinations for business travelers.

Munich is the third largest city in Germany and one of Europe's most prosperous. Munich has a population of about 1.3 million (as of 2006) and the Munich metropolitan area is home to around 2.7 million people.

The Bavarian Capital offers you a perfect combination for your private and business stay. Have you ever been at the „Wies'n"? The Munich Oktoberfest, the biggest public festival of the world, contains Bavarian Tradition, the new styled BMW Welt or the Allianz Arena, as one of the most modern soccer stadiums in Europe, are just some highlights in Munich, beside the Deutsche Museum, the Pinakotheken, the National Theater and our famous Castle Nymphenburg.

**See also: www.munich.de**

# Accommodation

The Munich Marriott Hotel offers everything you would expect from a first-class hotel. It claims to offer a little more feeling of being at home regardless of how far away from home you may be. All rooms are equipped with individual adjustable air-condition, color TV with inhouse movies, telephone with voice mail, cordless phone, safe, minibar, iron and ironing board as well as high-speed Internet access.

For edaForum attendees edacentrum has arranged the following special room rates, valid during the edaForum07, available only with bookings by fax or phone:

Single room EUR 135 (without breakfast)
Double room EUR 135 (without breakfast)
Breakfast will be charged separately at EUR 22,00 per person.

Please book your room by October 25, 2007, and mention "edaForum" as keyword. After October 25, the fixed quota of rooms for the edaforum07 is closed. We recommend that you book early as the hotel could be booked up very quickly when trade fairs are taking place.

The hotel booking form is available via www (s. below) and will be sent by e-mail together with the confirmation of registration. All participants are kindly asked to make their own hotel reservations directly:

Munich Marriott Hotel
Berliner Straße 93
80805 Munich
Germany
Phone: +49 89 36002-0
Fax: +49 89 36002-200

**See also: www.marriott.com/mucno**

**The hotel booking form is available at www.edacentrum.de/edaforum/hotel_reservation.pdf**

# Directions to Munich Marriott Hotel



### From A9 Nürnberg, A8 Stuttgart and Salzburg

Go to the highway crossing "München-Nord", from there take A9 southbound, direction Munich. At the end of the highway go over the bridge, take the first street on the right (Theodora Dombart Str.), turn the next right again (Berliner Str.). After 200 m you find the Marriott hotel is at the right hand side.

### From A95 Garmisch-Partenkirchen, A96 Lindau

At the end of the highway follow the direction "Mittlerer Ring/ West" and "A9 Nürnberg". Follow the city highway behind the Olympia Area and through the "Petueltunnel", after the entrance of the highway Nürnberg turn the first street right.

### From the Main Railway Station

Take the U4 or U5 to "Odeonsplatz", change to U6, direction "Garching-Hochbrück", leave the train at station "Nordfriedhof". Take the exit at the right hand side. Then at the newspaper shop turn right and take this exit. Walk down the pedestrian zone. It takes about 15 minutes.

### From the Airport

**By car**

Take the A92, direction Munich, at the highway crossing "Neufahrn" leave the A92 in direction A9 München, then s. above.

**By Lufthansa Airport bus**

Departure every 20 min. Terminal A, D and Central Area Bus terminal. Fee one way € 10.00 (round trip € 16.00) per person. Traveling time approx. 30 minutes to the station München-Nord (junction Isarring-Ungererstrasse). Walking distance to the hotel approx. 5 minutes.

**By taxi**

The ride will take about 30 minutes and will cost about € 55.00.

**By public transportation**

From the central area take S1 or S8 to Munich. At station "Marienplatz" change to U6, direction "Garching-Hochbrück". Proceed as written above. It will take about 60 minutes.

# Registration

| | | |
|---|---|---|
| **Registration:** | **until Oct. 26** | **until Nov. 9** |
| **edacentrum members*** | **EUR 470** | **EUR 520** |
| **Non-members** | **EUR 940** | **EUR 990** |

(All prices exclude 19 % Sales Tax.)

**Late registrations cannot be guaranteed and will be charged an additional fee of EUR 50 (plus 19 % Sales Tax).**

The edaForum07 participation fee includes forum, social event, trips and tours, 2x lunch, conference beverages and conference documents. This is an all-inclusive package. Items are not available separately.

Payment is possible by invoice or credit card: MasterCard, VISA or AMEX. (We need to have the "card verification code" for credit card transactions.)

* For information and conditions concerning membership at edacentrum see www.edacentrum.de/membership.html

**To register choose the registration online (s. below) or fax the registration form to +49 511 762 19695.**

**For further request please contact:**
edacentrum
Ms. Maren Sperber
Schneiderberg 32
30167 Hanover
Germany
Phone: +49 511 762-19699
E-mail: edaforum@edacentrum.de

Registrations are processed in the order they are received. Confirmation receipts will be sent via e-mail if an e-mail address is provided. Otherwise, confirmation letters are posted within 7 to 10 business days of processing. Please review your registration confirmation for accuracy.

The registration desk at the edaForum07 will be located in front of the conference rooms during edaForum07:
December 6, 8:00 am - 5:30 pm
December 7, 8:30 am - 9:30 am / 11:00 am - 2:00 pm

**Cancellation**
Cancellation (only by written request) is possible free of charge until November 16, 2007. Until November 23, 2007, half of the participation fee is retained. After this date the entire participation fee is due. A replacement for the registered participant with the same affiliation is possible at any time.

**Registration Deadline: November 9, 2007**
**www.edacentrum.de/edaforum/registration**

# Trips & Tours



**Bavarian State Opera**
The National Theater on the Max-Joseph-Platz houses the Bavarian State Opera. The State Opera seats 2,100 people. Five rows of stalls and the royal box overlook the circular auditorium. The classical opera house has an impressive exterior and a magnificent interior. The theater's ensemble has a long-standing tradition of excellence. While visiting the Bavarian State Opera experience the impressive interior, learn about the history of the building and enjoy the view from the royal box.

**See also: www.bayerische.staatsoper.de**

**The BMW World**
The BMW World embodies BMW in all dimensions. It unites tradition and innovation, emotion and precision, dynamism and aesthetics, exclusivity and openness. The unique architecture that is visible from outside is reflected consistently throughout the interior. Experience the fascinating new dimension during the guided tour and learn about the architectural highlights. The guided tour is only available in German language.

**See also: www.bmw-welt.com**

**Allianz Arena**
The Allianz Arena, opened in 2005 and home of the Munich clubs Bayern and TSV 1860, was designed purely as football stadium. It took less than three years to build this architecturally unique arena, which was built especially for the FIFA World Cup 2006. Here you find out all you need to know about Europe's state of the art stadium. The visit starts with a film on the development of the Allianz Arena. After that there is a guided tour taking in the changing rooms, the tunnel, the interior rooms, the press club, the upper tier and a pitchside visit. The visit of the Allianz Arena will only take place when there is no football match on Dec. 7, 2007.

**See also: www.allianz-arena.de**

**Friday, Dec. 7, 2007**
**2:00 pm — 5:30 pm**
**Meetingpoint at the Hotel reception**

**Beer and Oktoberfest Museum**
Here you will learn all about the history of beer, from the migration of nations to the monasteries, the brewing and the "purity" law of 1516, and the quality of Munich beer. The Oktoberfest also has a long history, beginning as a national holiday to celebrate the wedding of Ludwig I. with Princess Theresa von Sachsen-Hildburghausen and becoming in time the largest folk festival in the world.

**See also: www.bier-und-oktoberfestmuseum.de**

**BMW Munich Plant**
Visit the home plant of the BMW Group and experience live and in detail how BMW produce individual cars according to customer requirements with passion and precision. Experience how parts are produced from heavy coils of steel, how they are assembled into a car body and painted. See how an engine is produced. Follow a car on its way to completion, from the wedding of engine and car body to various quality tests. Experience the fascination of technology during a guided tour at the BMW Munich Plant.

**See also: www.bmw-werk-muenchen.de**

**Olympic Stadium**
For the 20th Summer Olympic Games in 1972, a former airfield in the north of Munich was transformed into a sports landscape with an artificial lake. During the guided tour you will be able to see she stadium from VIP lounges, hospitality areas, the changing rooms of the former World Champions, the VIP stands and the world-renowned hallowed turf. You can also prove your ability to score goals at the new 6 meter long Kicker table soccer, where 22 persons with 6 balls can play together.

**See also: www.olympiapark-muenchen.de**

**Friday, Dec. 7, 2007**
**2:00 pm — 5:30 pm**
**Meetingpoint at the Hotel reception**

# Bavarian Evening

Enjoy a typical Bavarian Dinner accompanied by Bavarian traditional music in the famous "Weisses Brauhaus" in the city of Munich.

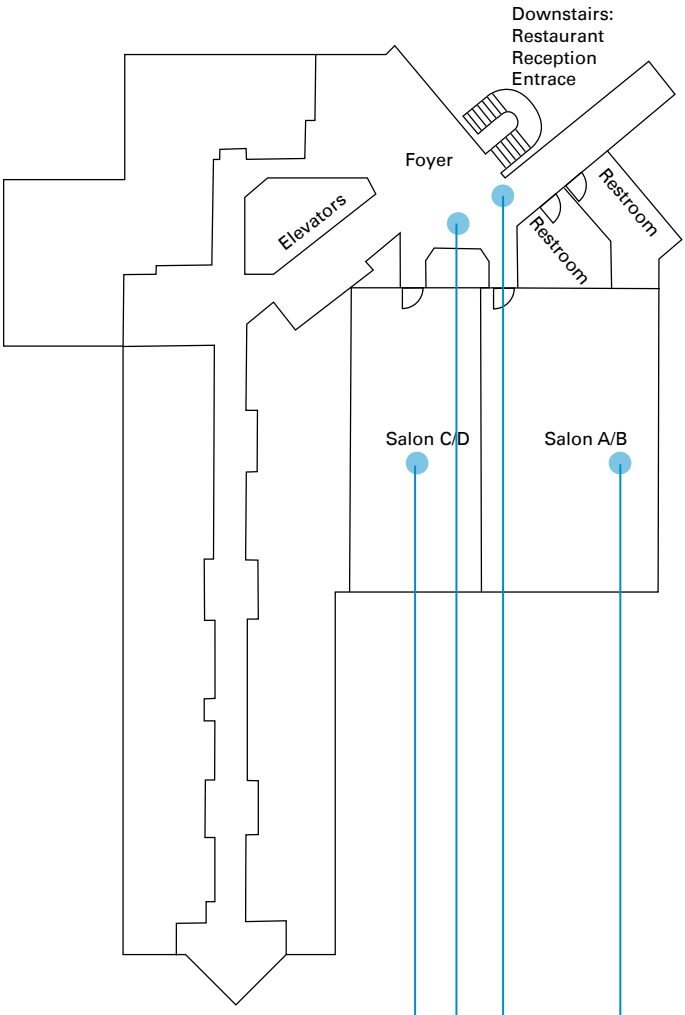
The "Weisses Brauhaus" in Munich is the founding place of the brewery "Schneider Weisse". It is the place where the founder of the company, Georg Schneider I., brewed his first Schneider Weisse Original in 1872. Now as before, it is regarded as one of the most beautiful and traditional beerhouses in this region.

The Social Event finalizes with a beer tasting where you have the possibility to taste the different varieties of Schneider Weisse.

**See also: www.weisses-brauhaus.de**

**Thursday, Dec. 6, 2007**
**7:00 pm – 11:00 pm**
**Weisses Brauhaus, Tal 7, near Marienplatz**

# Floor Plan of Munich Marriott Hotel




**Business Session:** Salon C/D

**Registration:** Foyer

**EDA Lounge:** Foyer

**Technical Session:** Salon A/B

**The edaForum is organized by**

edacentrum

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# About the past events

With the first five edaForum events (Hannover 2002 and 2005, Stuttgart 2003, Dresden 2004, Berlin 2006), edacentrum established an unique event for decision makers. The feedback from attendees emphasizes the outstanding networking opportunities, the top class speakers and the special focus:

**Aldo Romano, STMicroelectronics Italy:**
"What I liked most at the edaForum06 was the perfect organization and the value of participants: I found very stimulating the possibility of meeting in the same environment important customers, valuable competitors and the best software suppliers. Excellent organization in an impressive city."

**Alberto Sangiovanni-Vincentelli, University of California at Berkeley:**
"It was a real pleasure to participate to edaForum05 as I had an opportunity for interaction with key people in our industry in a vibrant environment. I particularly appreciated the mix of technical and business content that the workshop offers; a combination that is hard to find in existing conferences and workshops."

**Tom DeMarco, Principal of The Atlantic Systems Guild:**
"The 2004 edaForum was the first I've attended, and I came away very impressed. The quality of the networking at this event was unmatched. The interaction among attendees was frank and extremely useful. Of the many conferences I regularly attend, I can't think of any which surpasses edaForum in establishing an active and sharing community of interest."

# Thursday, Dec. 6, 2007

8:30 am **Come Together**

## Company Presentations

Salon A/B

9:00 am **Martin Radetzki, University of Stuttgart:**
**"Metrics for productivity and how to use them?"**

9:40 am **Panel:**
**"Metrics and Tools for Improving Chip Design Productivity"**
Panelists represent the leading companies in the EDA industry
Moderator: Jürgen Haase, edacentrum

10:30 am **Coffee Break**
**Exhibition:**
**EDA vendors present their approaches for improving chip design productivity, on posters and with demos.**

12:00 pm **Lunch**

## Welcome Address

1:00 pm Salon A/B

Erich Barke, edacentrum

## General Keynote

1:15 pm Salon A/B

**Hermann Eul, Executive Vice President Infineon:**
**"Beyond IC Design -**
**Challenges for the Next Generation of EDA Software"**

## Technical Session I

"STILL HAVEN'T FOUND WHAT I'M LOOKING FOR"
**Mixed Signal Integration: All done?**

Chairman: Erich Barke

**Keynote** Salon A/B

2:20 pm **Georges Gielen, U Leuven:**
**"Analog Design Automation: Dream or Reality?"**

3:05 pm **Coffee Break**

3:35 pm **Werner Geppert, Infineon:**
**"RF & MS Integration Challenges in Single Chips for Mobile Phone Applications"**

4:05 pm **Oscar Buset, Kimotion:**
**"Analog Design Tools for Nanometer Processes"**

4:35 pm **Wolfgang Fichtner, Synopsys:**
**"Breaking Down the Manufacturing Design Firewall - DFM Flows are Becoming Reality"**

## Business Session I

"WOULDN'T IT BE NICE"

**Microelectronics Meets Medicine**

Chairman: Dirk Friebel

**Keynote** Salon C/D

**Bernhard Wolf, TU Munich:**
**"Microelectronics Meets Medicine ($m^3$): Electronic Systems for Diagnosis and Therapy"**

**Bernd Flick, TU Berlin:**
**"A Microelectronic Telemetrical Measurement System for Intracranial Pressure and Temperature"**

**Thomas Schweizer, Aipermon:**
**"Innovations in Telemedicine"**

**Matthias Schönermark, Hannover Medical School:**
**"Economical and Strategic Aspects of Medical Innovation Markets"**

5:05 pm **Break**

## Social Event

7:00 pm Weisses Brauhaus

**Bavarian Evening**
6:15 pm: Departure at the Hotel reception

# Friday, Dec. 7, 2007

## Technical Session II

"LET'S STICK TOGETHER"
**Hardware and Software Team up!**

Chairman: Wolfgang Rosenstiel

**Keynote** Salon A/B

9:00 am **Mikko Terho, Nokia:**
**"Are EDA tools for Systems Architecture, ASIC Design or Agile Software Development"**

9:40 am **Stefan Koerner, IBM:**
**"Virtual Power on in IBM"**

**Coffee Break** 10:05 am

10:35 am **Hans-Christian Reuss, FKFS:**
**"Challenges in Testing Electronic Control Units for the Automobile"**

11:00 am **Jean-Marie Saint-Paul, Mentor Graphics:**
**"Why should Hardware Designers have a Drink with Software Teams?"**

## Business Session II

"I WILL SURVIVE"
**Semiconductor Industry Consolidation: How Many Will Survive?**

Chairman: Peter van Staa

**Keynote** Salon C/D

9:00 am **G. Dan Hutcheson, VLSI Research:**
**"Semiconductor Industry Consolidation: Who will survive?"**

9:40 am **Craig Johnson, Cadence:**
**"Solutions for Enterprise Product Development"**

10:35 am **Thilo von Selchow, ZMD:**
**"Transformation of an East German Technology Portfolio into a Medium-Sized Global 'Fabless Company' in the Analog Mixed Signal Segment"**

11:00 am **Josef Winnerl, Infineon:**
**"Smart Technology Access - How to Position in the Semiconductor Value Chain"**

## Panel Discussion

11:30 am Salon A/B

**"Will consolidation in semiconductor industry and software dominated chip designs turn the EDA market upside down?"**
Moderator: Wolfgang Rosenstiel, edacentrum

12:30 pm **Lunch**

## Trips & Tours

2:00 pm – 5:30 pm

**Detailed information on page 28/29**

Foyer

**Registration Opening Time**

**1st day:** 8:00 am – 5:30 pm
**2nd day:** 8:30 am – 9:30 am & 11:00 am – 2:00 pm

## EDA Lounge

Foyer

Aiming to create an area for communication in a relaxed atmosphere, the EDA Lounge will be a meeting place inviting to talk to colleagues, partners and company representatives. The EDA Lounge will accompany the whole event.