Design for Manufacturing in Extreme Scaling and Beyond

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Invited Presentation - Abstract

As the nanometer IC critical dimension enters the era of extreme scaling (14nm, 11nm and beyond), manufacturability challenges are exacerbated, due to multiple patterning and other emerging lithography technologies. Meanwhile, the vertical scaling with 3D-IC integration using through-silicon-vias (TSVs) has gained tremendous interest and initial industry adoption, but TSV involves disruptive manufacturing technologies that require new modeling and design techniques for reliable 3D IC integration. All these require new design and process technology co-optimizations. This talk will present some key challenges and recent results in design for manufacturing in extreme scaling and beyond. Cross-layer modeling, CAD tool, and methodologies will be discussed, including multiple patterning lithography (MPL) layout decomposition, MPL standard cell compliance and placement composability, manufacturing hotspot detection using machine learning, and full-chip/package TSV stress modeling and 3D-IC DFM issues.

Curriculum Vitae

 David Z. Pan received his BS degree from Peking University, and MS/PhD degrees from UCLA. He was a Research Staff Member at IBM T. J. Watson Research Center from 2000 to 2003. He is currently the Engineering Foundation Professor at the Department of Electrical and Computer Engineering, UT Austin. He has published over 200 refereed journal and conference papers. He has served in many journal editorial boards (TCAD, TVLSI, TCAD-I, TCAS-II, TODAES, SCIS, JCST, etc.) and conference organizing/program committees (DAC, ICCAD, ASPDAC, ISLPED, ISPD, etc.). He is a working group member of the *International Technology Roadmap for Semiconductor* (ITRS). He has received a number of awards, including the SRC 2013 Technical Excellence Award, DAC Top 10 Author in Fifth Decade, DAC Prolific Author Award, ASP-DAC Frequently Cited Author Award, 11 Best Paper Awards (ISPD 2014, ICCAD 2013, ASPDAC 2012, ISPD 2011, IBM Research 2010 Pat Goldberg Memorial Best Paper Award in CS/EE/Math, ASPDAC 2010, DATE 2009, ICICDT 2009, SRC Techcon in 1998, 2007 and 2012), Communications of the ACM Research Highlights (2014), ACM/SIGDA Outstanding New Faculty Award (2005), NSF CAREER Award (2007), SRC Inventor Recognition Award three times, IBM Faculty Award four times, UCLA Engineering Distinguished Young Alumnus Award (2009), ISPD Routing Contest Awards (2007), eASIC Placement Contest Grand Prize (2009), ICCAD'12 and ICCAD'13 CAD Contest Awards, among others. He is an IEEE Fellow.