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2024/12/20

FastPath: A Hybrid Approach for Efficient Hardware Security Verification, Lucas Deutschmann1, Andres Meza2, Dominik Stoffel1, Wolfgang Kunz1, and Ryan Kastner2; 1RPTU Kaiserslautern-Landau, 2UC San Diego; 62th IEEE/ICM Design Automation Conference (DAC), San Francisco, USA, 2025.

Paul Palomero Bernardo, Patrick Schmid, Christoph Gerum, and Oliver Bringmann. 2025. Compiler-aware AI Hardware Design for Edge Devices. In The 8th International Workshop on Edge Systems, Analytics and Networking (EdgeSys '25), March 30-April 3, 2025, Rotterdam, Netherlands. ACM, New York, NY, USA, 6 pages. https://doi.org/10.1145/3721888.3722095

Towards Non-Intrusive SystemC Checkpointing for Digital Virtual Prototypes, Deepak Ravibabu (1), Muhammad Hassan <hassan@uni-bremen [dot] de> (1,3), Thilo Vörtler (2), Karsten Einwich (2), Rolf Drechsler (1,3), and Daniel Große (1,4); (1) Cyber-Physical Systems, DFKI GmbH, 28359 Bremen, Germany, (2) COSEDA Technologies GmbH, 01099 Dresden, Germany, (3) Institute of Computer Science, Bremen University, 28359 Bremen, Germany, (4) Institute for Complex Systems, Johannes Kepler University, 4040 Linz, Austria, MBMV-Workshop, 11.03.2025, Rostock, DE.

Symbolic Execution of Unmodified SystemC Peripherals, Karl Aaron Rudkowski <karlaaron@uni-bremen [dot] de> (1) , Sallar Ahmadi-Pour (1) , and Rolf Drechsler (1,2), (1) Institute of Computer Science, University of Bremen, Germany, (2) Cyber-Physical Systems, DFKI GmbH, Bremen, Germany, MBMV-Workshop, 11.03.2025, Rostock, DE.

Improving Design Generation by Interface Configuration Propagation Natalie Simson, Infineon Technologies AG and Technical University of Munich, DE, <natalie [dot] simson@infineon [dot] com>, Paritosh Kumar Sinha, Infineon Technologies AG, DE, Wolfgang Ecker, Infineon Technologies AG and Technical University of Munich, DE, MBMV-Workshop, 11.03.2025, Rostock, DE.

Platform-Aware RTL Generation: Bridging the Gap between Design and Implementation Mohamed Badawy, Infineon Technologies AG, DE <mohamed [dot] badawy@infineon [dot] com>, Nicolas Gerlin, Paritosh Kumar Sinha, Endri Kaja, Jad Al Halabi, Stephanie Ecker, Natalie Simson, Wolfgang Ecker, Infineon Technologies AG and Technical University of Munich, DE, MBMV-Workshop, 11.3.2025, Rostock, DE.

Parameterized Construction and Constraint-Driven Validation of Formal Hardware Specifications for Efficient Code Generation, Robert Kunzelmann, Infineon Technologies AG and Technical University of Munich, DE <robertniklas [dot] kunzelmann@infineon [dot] com>, Maximilian Berger, Infineon Technologies AG, DE and and Technical University of Munich, DE, Wolfgang Ecker, Infineon Technologies AG and Technical University of Munich, DE, MBMV-Workshop, 11.3.2025, Rostock, DE.

Verilator and FireSim RTL Simulations on a HPC Cluster: A Comparative Case Study, Kai Hannemann, Universität Paderborn, DE <kaiha@hni [dot] uni-paderborn [dot] de>, Hüseyin Berke Bütün, Wolfgang Mueller, Christoph J. Scheytt, MBMV-Workshop, 11.3.2025, Rostock, DE.

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VeriCHERI: Exhaustive Formal Security Verification of CHERI at the RTL, Anna Lena Duque Antón∗, Johannes Müller∗, Philipp Schmitz, Tobias

Jauch, Alex Wezel, Lucas Deutschmann, Mohammad R. Fadiheh, Dominik Stoffel, Wolfgang Kunz, RPTU Kaiserslautern-Landau, ∗Both authors contributed equally to this research, ICCAD 2024, October 27–31, 2024, New York, NY, USA

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SIZALIZER: Multilevel Analysis Framework for Object Size Optimization, Andreas Hager-Clukas, Jonathan Schröter, and Stefan Wallentowitz, Hochschule München University of Applied Sciences, International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation (SAMOS), June 29 - July 4, 2024.

MCU-Wide Timing Side Channels and Their Detection, Johannes Müller1, Anna Lena Duque Antón1, Lucas Deutschmann1, Dino Mehmedagić1, Cristiano Rodrigues2, Daniel Oliveira2, Keerthikumara Devarajegowda3, Mohammad Rahmani Fadiheh4, Sandro Pinto2, Dominik Stoffel1, and Wolfgang Kunz1 1RPTU Kaiserslautern-Landau, 2Universidade do Minho, 3Siemens EDA, 4Stanford University, DAC 2024

Unique Program Execution Checking: Formal Security Guarantees for RISC-V Systems, Alex Wezel, Lucas Deutschmann, Tobias Jauch, Dino Mehmedagić, Johannes Müller, Mohamed Ali, Anna Lena Duque Antón, Philipp Schmitz, Mohammad Rahmani Fadiheh, Dominik Stoffel, Wolfgang Kunz, Übersichtsvortrag, RISC-V Summit Europe 2024, 24.-28.6.2024, München

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Cross-Level Verification of Hardware Peripherals, Sallar Ahmadi-Pour1, Muhammad Hassan1,2, Rolf Drechsler1,2 *, 1Institute of Computer Science, University of Bremen, Germany, 2Cyber-Physical Systems, DFKI GmbH, Germany, RISC-V Summit Europe 2024, Munich, Germany 24-28 June 2024.

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A Universal Specification Methodology for Quality Ensured, Highly Automated Generation of Design Models; Robert Kunzelmann1, 2, Emil Baerens1, Daniel Gerl1, 2, Mayuri Bhadra1, 2, Niklas Schwarz1, and Wolfgang Ecker1, 2; 1Infineon Technologies AG, Neubiberg, Germany; 2Technical University of Munich, Munich, Germany, MBMV 2024, 14.+15.2.2024, Kaiserslautern, Germany

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Extending Clang/LLVM with Custom Instructions using TableGen – An Experience Report; Jan Schlamelcher, Thomas Goodfellow, Bewoayia Kebianyor, and Kim Grüttner, German Aerospace Center - Institute of Systems Engineering for Future Mobility, MBMV 2024, 14.+15.2.2024, Kaiserslautern, Germany

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A Concise, Architecture-Focused ASIP Modeling Approach for Instruction Set Simulators; Karsten Emrich, Daniel Mueller-Gritschneder, Ulf Schlichtmann, Chair of Electronic Design Automation, Technical University of Munich, MBMV 2024, 14.+15.2.2024, Kaiserslautern, Germany

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muRISCV-NN: Challenging Zve32x Autovectorization with TinyML Inference Library for RISC-V Vector Extension, Philipp van Kempen1, Jefferson Parker Jones1, Daniel Mueller-Gritschneder2, Ulf Schlichtmann1, 1Technical University of Munich, 2Vienna University of Technology, CF24-OSHW, Workshop on Open-Source Hardware, Co-located with 21th ACM International Conference on Computing Frontiers (CF’ 24) May 7 - May 9, 2024 - Ischia (NA), Italy

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Longnail: High-Level Synthesis of Portable Custom Instruction Set Extensions for RISC-V Processors from Descriptions in the Open-Source CoreDSL Language, Julian Oppermann1, Brindusa Mihaela Damian-Kosterhon1, Florian Meisel1, Tammo Mürmann1, Eyck Jentzsch2, Andreas Koch1, 1Technical University of Darmstadt, 2MINRES Technologies Munich, International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), https://www.asplos-conference.org/asplos2024/ [3], San Diego, USA — April 27- May 1, 2024

Data-Oblivious and Performant: On Designing Security-Conscious Hardware, Lucas Deutschmann∗, Yazan Kazhalawi∗, Jonathan Seckinger∗, Anna Lena Duque Antón∗, Johannes Müller∗, Mohammad Rahmani Fadiheh†, Dominik Stoffel∗, Wolfgang Kunz∗; ∗RPTU Kaiserslautern-Landau, Kaiserslautern, Germany †Stanford University, Stanford, US, LATS 2024; Maceió, BR, https://cas.polito.it/LATS2024/program

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TUDD Demo: ZuSE Scale4Edge – AI Hardware Accelerator for Ultra-Low-Power Keyword Spotting, ADTC + edaWorkshop24, Dresden, 9.+11.4.2024

Ein KI-Hardware-Beschleuniger für ultra-energieeffiziente Schlüsselworterkennung wird demonstriert. Durch Optimierung der Vorverarbeitung, Ausnutzung von Sparsity in einem Beschleuniger für rekurrente neuronale Netzwerke sowie einen hierarchischen Aufwachmechanismus erreichen wir eine sehr niedrige Leistungsaufnahme bei gleichzeitig hoher Klassifikationsgüte.

IHP Demo: ZuSE Scale4Edge – Der TETRISC SoC - unser RISC-V-basiertes, fehlertolerantes Mehrkernsystem auf FPGA und gefertigt als ASIC, ADTC + edaWorkshop24, Dresden, 9.+11.4.2024

Unser Demonstrator präsentiert zwei Ausführungen des adaptiven und fehlertoleranten TETRISC SoC. Zum einen umfasst er eine prototypische Implementierung auf FPGA, mit der wir gezielt Fehler einspeisen können, um die Fehlertoleranz des Systems zu demonstrieren. Zum anderen präsentieren wir die finale Version, gefertigt in IHP 130nm Technologie. Diese zeigt die Realisierbarkeit und Funktionalität des Systems und ermöglicht Messungen zur Geschwindigkeit und Stromaufnahme.

UFR Demo: ZuSE Scale4Edge – Software-based Self-Test Generation for RISC-V, FPGA-basierter Demonstrator

Ein FPGA-basierter Demonstrator mit einem RISC-V Prozessorkern, welcher die LED-Anzeigen auf der Demoplatine steuert und periodisch einen Selbsttest ausführt. Die SBST ist für den Test der Arithmetic Logic Unit (ALU) und die Registerbank des verwendeten RISC-V Prozessorkernes ausgelegt. Über Schalter können ausgewählte Fehler in den Prozessorkern injiziert werden, welcher dann mittels des SBSTs diese detektiert, und auf den Anzeigen das Testergebnis signalisiert.

Poster: Trust & Security-Forschungen in Scale4Edge und VE-VIDES durch die Werkzeuge Questa Verify Secure und Questa Verify Trust, Jörg Bormann, Siemens EDA, ADTC + edaWorkshop24, Dresden, 9.+11.4.2024

TUDD-Poster: AI Hardware Accelerator for Ultra-Low-Power Keyword Spotting, Johannes Partzsch, TU Dresden, ADTC + edaWorkshop24, Dresden, 9.+11.4.2024

TUDD-Demo: AI Hardware Accelerator for Ultra-Low-Power Keyword Spotting, Johannes Partzsch, TU Dresden, ADTC + edaWorkshop24, Dresden, 9.+11.4.2024

A Golden-Free Formal Method for Trojan Detection in Non-Interfering Accelerators, Anna Lena Duque Antón1, Johannes Müller1, Lucas Deutschmann1, Mohammad Rahmani Fadihehy2, Dominik Stoffel1, Wolfgang Kunz1; 1University of Kaiserslautern-Landau, Kaiserslautern, Germany 2Stanford University, Stanford, USA, DATE 2024

A Scalable RISC-V Hardware Platform for Intelligent Sensor Processing; Paul Palomero Bernardo, Patrick Schmid, Oliver Bringmann, University of Tübingen, Mohammed Iftekhar, Babak Sadiye, Wolfgang Müller Paderborn University / Heinz Nixdorf Institute, Andreas Koch, Technical University of Darmstadt, Eyck Jentzsch, MINRES Technologies GmbH, Axel Sauer, Ingo Feldner, Robert Bosch GmbH, Wolfgang Ecker, Infineon Technologies AG; 25.-27.3.2024 at Design, Automation and Test in Europe (DATE) Conference 2024, Valencia, ES (https://date24.date-conference.com/programme [4]).

A Scalable Formal Verification Methodology for Data-Oblivious Hardware, Lucas Deutschmann1, Johannes Müller1, Mohammad R. Fadiheh2, Dominik Stoffel1, and Wolfgang Kunz1; 1University of Kaiserslautern-Landau, Kaiserslautern, Germany 2Stanford University, Stanford, USA, TCAD 2024; https://doi.org/10.1109/TCAD.2024.3374249

J. Kappes, R. Kunzelmann, K. Emrich, C. Foik, D. Mueller-Gritschneder and W. Ecker, Effective Processor Model Generation from Instruction Set Simulator to Hardware Design, 2023 IEEE Nordic Circuits and Systems Conference (NorCAS), Aalborg, Denmark, 2023, pp. 1-7, https://doi.org/10.1109/NorCAS58970.2023.10305465.

A RISC-V MCU with adaptive reverse body bias and ultra-low-power retention mode in 22 nm FD-SOI; Heiner Bauer, Marco Stolba, Stefan Scholze, Dennis Walter, Christian Mayr, Electrical and Computer Engineering Dept., TU Dresden, Germany, Alexander Oefelein, Sebastian Höppner, André Scharfe, Flo Schraut, Holger Eisenreich, Racyics GmbH, Dresden, Germany, 20th International SoC Conference (ISOCC 2023) will be held from October 25 to 28, 2023 at at the Ramada Plaza Jeju Hotel in Jeju Island, Korea, https://isocc.org.

N. I. Deligiannis, T. Faller, I. Guglielminetti, R. Cantoro, B. Becker, M. S. Reorda, Automatic Identification of Functionally Untestable Cell-Aware Faults in Microprocessors, to be published on 2023 IEEE 32nd Asian Test Symposium (ATS), October 14-17, 2023, Beijing, China

Minimally Invasive Generation of RISC-V Instruction Set Simulators from Formal ISA Models; Sören Tempel1 Tobias Brandt Christoph Lüth1,2 Rolf Drechsler1,2; 1Institute of Computer Science, University of Bremen, Germany; 2Cyber-Physical Systems, DFKI GmbH, Bremen, Germany; FDL 2023

Virtual Prototype driven Application Specific Hardware Optimization; Jan Zielasko1 Rolf Drechsler1,2; 1Cyber-Physical Systems, DFKI GmbH, Germany; 2Institute of Computer Science, University of Bremen, Germany; FDL 2023

Identification of ISA-Level Mutation-Classes for Qualification of RISC-V Formal Verification, Milan Funck1 Sallar Ahmadi-Pour2 Vladimir Herdt1,2 Rolf Drechsler1,2; 1Cyber-Physical Systems, DFKI GmbH, Bremen, Germany; 2Institute of Computer Science, University of Bremen, Bremen, Germany; FDL 2023

A RISC-V based platform supporting mixed timing-critical and high performance workloads, Mehrdad Poorhosseini, University of Oldenburg, Kim Grüttner, German Aerospace Center (DLR), 26th Euromicro Conference on Digital System Design (DSD) in Durres, Albania, Sept. 6th – Sept. 8th, 2023.

Efficient ML-Based Performance Estimation Approach across Different Microarchitectures for RISC-V Processors, Weiyan Zhang1 Mehran Goli2 Muhammad Hassan1,2 Rolf Drechsler1,2, 1Cyber-Physical Systems, DFKI GmbH, 2Institute of Computer Science, University of Bremen, 26th Euromicro Conference on Digital System Design (DSD) in Durres, Albania, Sept. 6th – Sept. 8th, 2023.

The TETRISC SoC - A resilient Quad-Core System based on the ResiliCell approach, Markus Ulbricht a, Li Lu a, Junchao Chen a, Milos Krstic a b, a IHP - Leibniz Institute for High Performance Microelectronics, b University of Potsdam, Received 2 June 2023, Revised 24 July 2023, Accepted 28 July 2023, Available online 14 August 2023, Version of Record 14 August 2023., Microelectronics Journal, https://doi.org/10.1016/j.microrel.2023.115173.

Design of Access Control Mechanisms in Systems-on-Chip with Formal Integrity Guarantees; Dino Mehmedagić, Mohammad Rahmani Fadiheh, Johannes Müller, Anna Lena Duque Antón, Dominik Stoffel, Wolfgang Kunz, Department of Electrical and Computer Engineering, Rheinland-Pfälzische Technische Universität (RPTU) Kaiserslautern-Landau, Germany, 32nd USENIX Security Symposium, 9.-11.8.2023, in Anaheim, CA, USA

RISC-V Timing-Instructions for Open Time-Triggered Architectures, Nithin Ravani Nanjundaswamy, Gregor Nitsche, Frank Poppen (now: NXP Semiconductors Germany GmbH, Hamburg), Kim Grüttner, German Aerospace Center, Oldenburg, Germany, VERDI 2023, 1st International Workshop on Verification & Validation of Dependable Cyber-Physical Systems, 27 June 2023, Porto, Portugal, Co-located with DSN 2023

Liyuan Guo, Matthias Jobst, Johannes Partzsch, Stefan Scholze, Andreas Dixius, Matthias Lohrmann, Seyed Mohammad Ali Zeinolabedin, Christian Mayr: A Low-Power Hardware Accelerator of MFCC Extraction for Keyword Spotting in 22nm FDSOI, Konferenz „Artificial Intelligence Circuits and Systems“ (AICAS) 2023

The TETRISC SoC - A resilient quad-core system based on Pulpissimo, Markus Ulbricht1, Junchao Chen1, Li Lu1 and Milos Krstic1,2, 1IHP - Leibniz Institute for High Performance Microelectronics, Frankfurt (Oder), Germany, 2University of Potsdam, Potsdam, Germany, RISC-V Summit Europe 2023, Barcelona, Spain, 5.-9.6.2023

Automated Cross-level Verification Flow of a Highly Configurable RISC-V Core Family with Custom Instructions, Stanislaw Kaushanski, Eyck Jentzsch, MINRES Technologies GmbH, Germany, RISC-V Summit Europe 2023, Barcelona, Spain, 5.-9.6.2023

Scale4Edge – Scaling RISC-V for Edge Applications, Wolfgang Ecker1, Milos Krstic2,3, Markus Ulbricht2, Andreas Mauderer4, Eyck Jentzsch5, Andreas Koch6, Bastian Koppelmann7, Wolfgang Mueller7, Babak Sadiye7, Niklas Bruns8, Rolf Drechsler8, Daniel Mueller-Gritschneder9, Jan Schlamelcher10, Kim Grüttner10, Jörg Bormann11, Wolfgang Kunz12, Reinhold Heckmann13, Gerhard Angst14, Ralf Wimmer14, Bernd Becker15, Tobias Faller15, Paul Palomero Bernardo16, Oliver Bringmann16, Johannes Partzsch17, Christian Mayr17, 1Infineon Technologies AG, 2IHP – Leibniz Institut für innovative Mikroelektronik, 3University Potsdam, 4Robert Bosch GmbH, 5MINRES Technologies GmbH, 6Technical University of Darmstadt, 7Heinz Nixdorf Institute/Paderborn University, 8University of Bremen / DFKI GmbH, 9Technical University of Munich, 10German Aerospace Center (DLR), 11Siemens EDA, 12Technische Universität Kaiserslautern, 13AbsInt Angewandte Informatik GmbH, 14Concept Engineering GmbH, 15Albert-Ludwigs-Universität Freiburg, 16Universität Tübingen, 17Technische Universität Dresden, RISC-V Summit Europe 2023, Barcelona, Spain, 5.-9.6.2023

Extended Abstract: Automated Generation of a RISC-V LLVM Toolchain for Custom MACs, Philipp van Kempen1∗, Karsten Emrich1, Daniel Mueller-Gritschneder1 and Ulf Schlichtmann1, 1School of Computation, Information and Technology, Technical University of Munich, RISC-V Summit Europe 2023, Barcelona, Spain, 5.-9.6.2023

Extended Abstract: A Flexible Simulation Environment for RISC-V, Karsten Emrich1, Conrad Foik1, Johannes Kappes2, Sebastian Prebeck2, Daniel Mueller-Gritschneder1, Wolfgang Ecker2, Ulf Schlichtmann1, 1Technical University of Munich, Germany 2Infineon Technologies, RISC-V Summit Europe 2023, Barcelona, Spain, 5.-9.6.2023

T. Faller, N. Deligiannis, M. Schwörer, M. S. Reorda, B. Becker, Constraint-Based Automatic SBST Generation for RISC-V Processor Families, 28th IEEE European Test Symposium 2023, 22-26 May 2023, Venezia, Italy

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PULP Fiction No More - Dependable PULP Systems for Space; Markus Ulbricht∗, Yvan Tortorella†, Michael Rogenmoser‡, Li Lu∗, Junchao Chen∗, Francesco Conti†, Milos Krstic∗§, Luca Benini†‡; ∗IHP - Leibniz Institute for High Performance Microelectronics, DE, †DEI Department, University of Bologna, IT, ‡Integrated Systems Laboratory (IIS), ETH Zürich, CH, §University of Potsdam, Potsdam, DE at 28th IEEE European Test Symposium (ETS) 2023 on May 22-26 in Venice, IT

A Survey of Recent Developments in Testability, Safety and Security of RISC-V Processors; Jens Anders, Pablo Andreu, Bernd Becker, Steffen Becker, Riccardo Cantoro, Nikolaos I.Deligiannis, Nourhan Elhamawy, Tobias Faller, Carles Hernandez, Nele Mentens, Mahnaz Namazi Rizi, Ilia Polian, Abolfazl Sajadi, Mathias Sauer, Denis Schwachhofer, Matteo Sonza Reorda, Todor Stefanov, Ilya Tuzov, Stefan Wagner and Nuša Zidarič; 2023 IEEE European Test Symposium (ETS), Venezia, Italy, 2023, pp. 1-10, https://doi.org/10.1109/ETS56758.2023.10174099.

Constraint-Based Automatic SBST Generation for RISC-V Processor Families; Tobias Faller∗, Nikolaos I. Deligiannis†, Markus Schwörer∗, Matteo Sonza Reorda†, Bernd Becker∗, ∗University of Freiburg, Department of Computer Science - Freiburg, Germany, †Politecnico di Torino, Department of Control and Computer Engineering (DAUIN) - Turin, Italy, ETS 2023

Efficient Software-Implemented HW Fault Tolerance for TinyML Inference in Safety-critical Applications; Uzair Sharif, Daniel Mueller-Gritschneder, Rafael Stahl, Ulf Schlichtmann, Chair of Electronic Design Automation, Technical University of Munich (TUM), Munich, Germany at Design, Automation and Test in Europe (DATE) Conference 2023, Antwerp, BE

Best Paper Award Candidate: Processor Verification using Symbolic Execution: A RISC-V Case-Study; Niklas Bruns, Vladimir Herdt and Rolf Drechsler; Universität Bremen, Design, Automation and Test in Europe (DATE) Conference 2023, Antwerp, BE

Fused Depthwise Tiling for Memory Optimization in TinyML Deep Neural Network Inference; Rafael Stahl, Daniel Mueller-Gritschneder, Ulf Schlichtmann, Technical University of Munich, Germany, TinyML Research Symposium 2023

Luchterhandt, Lars; Nellius, Tom; Beck, Robert; Dömer, Rainer; Kneuper, Pascal; Mueller, Wolfgang; Sadiye, Babak. Towards a Rocket Chip Based Implementation of the RISC-V GPC Architecture. In: Workshop Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen (MBMV 2023), IEEE Xplore, 18. - 19. Mrz. 2023.

N. I. Deligiannis, T. Faller, R. Cantoro, T. Paxian, B. Becker and M. S. Reorda, Automating the Generation of Programs Maximizing the Repeatable Constant Switching Activity in Microprocessor Units via MaxSAT, in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, https://doi.org/10.1109/TCAD.2023.3252467.

Specification-based Symbolic Execution for Stateful Network Protocol Implementations in the IoT. Sören Tempel, Vladimir Herdt, Rolf Drechsler, IEEE Internet of Things Journal 2023; https://doi.org/10.1109/JIOT.2023.3236694

Versatile and Flexible Modelling of the RISC-V Instruction Set Architecture; Sören Tempel1, Tobias Brandt3, and Christoph Lüth1,2; 1University of Bremen, DE; 2Deutsches Forschungszentrum für Künstliche Intelligenz (DFKI), DE; 3tobbra91@gmail [dot] com; TFP (and TFPIE) 2023, 24th International Symposium on Trends in Functional Programming, 12 - 15 January 2023, UMass Boston, Boston, MA, USA; https://trendsfp.github.io/schedule.html

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Präsentation: OPTI-RISK: Design of an Optical Probing Attack Hardened RISC-V Core with an Industrially Compatible CMOS Gate Library. Sajjad Parvin, Sallar Ahmadi-Pour, Chandan Kumar Jha, Frank Sill Torres, and Rolf Drechsler. 5th RISC-V Activity Workshop 2022

Schlamelcher, Jan und Grüttner, Kim (2022) A DSL based approach for supporting custom RISC-V instruction extensions in LLVM. 5th Workshop on RISC-V Activities, Berlin, Deutschland.

Ravani Nanjundaswamy, Nithin und Grüttner, Kim (2022) Timing-Anweisungen für RISC-V-basierte Hard Real Time Edge Devices 5th Workshop on RISC-V Activities, Berlin, Deutschland.

Wolfgang Kunz: „Spectres, Meltdowns, Zombies, Orcs: Can formal methods banish the ghosts that haunt your hardware?” Keynote; 5th Workshop on RISC-V Activities, Berlin, Germany, 7.11.2022

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Vladimir Herdt, Sören Tempel, Daniel Große, and Rolf Drechsler; Mutation-based Compliance Testing for RISC-V; In 26th Asia and South Pacific Design Automation Conference (ASPDAC '21), January 18–21, 2021, Tokyo, Japan. ACM, New York, NY, USA, 6 pages. https://doi.org/10.1145/3394885.3431584

RISC-V Summit 2020 with "Scale4Edge project introduction" by Wolfgang Ecker, Lead Principle Engineer, Infineon Technologies, Virtual Event, Tuesday, 8 December 2020 12:00pm - 12:20pm - PST (Pacific Standard Time, GMT-8); https://tmt.knect365.com/risc-v-summit/

Vortrag auf der Onespin User-Konferenz OSMOSIS 2020: W. Kunz: "Hardware Security Verification using Unique Program Execution Checking", 1.-2.12.2020, (virtuell).

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Herdt, V., Große, D., Drechsler, R. (2020). RVX - A Tool for Concolic Testing of Embedded Binaries Targeting RISC-V Platforms. In: Hung, D.V., Sokolsky, O. (eds) Automated Technology for Verification and Analysis. ATVA 2020. Lecture Notes in Computer Science(), vol 12302. Springer, Cham. https://doi.org/10.1007/978-3-030-59152-6_31

Security Issues in Hardware/Firmware interaction – Can a formal analysis of (just) the hardware help?, Johannes Müller (Technical University of Kaiserslautern, D), Workshop on RISC-V Activities 2020, 8.10.2020, Virtuell

A Configurable Virtual Prototyping Environment for Different RISC-V ISA Subsets, Peer Adelt (University of Paderborn, D), Workshop on RISC-V Activities 2020, 8.10.2020, Virtuell

Efficient RISC-V Processor Verification via Cross-Level Testing, Vladimir Herdt (University of Bremen / DFKI, D), Eyck Jentzsch (MINRES Technologies, D), Daniel Große (Johannes Kepler University Linz, AT), Rolf Drechsler (University of Bremen / DFKI, D), Workshop on RISC-V Activities 2020, 8.10.2020, Virtuell

A Compiler Comparison in the RISC-V Ecosystem, Mehrdad Poorhosseini, Kim Grüttner, Wolfgang Nebel (OFFIS, D), Workshop on RISC-V Activities 2020, 8.10.2020, Virtuell

Energy Efficient RISC-V Implementations in 22 nm, Heiner Bauer (Technical University of Dresden, D), Workshop on RISC-V Activities 2020, 8.10.2020, Virtuell

A RISC-V based Edge Computing Platform with Interchangeable Cores Using 22FDX, Paul Palomero Bernardo, Adrian Frischknecht, Dustin Peterson, University of Tuebingen, D, Workshop on RISC-V Activities 2020, 8.10.2020, Virtuell

Keynote: RISC-V Scale4Edge Ecosystem - Motivation and Objectives, Wolfgang Ecker (Infineon, D), Workshop on RISC-V Activities 2020, 8.10.2020, Virtuell

UltraTrail: A Configurable Ultralow-Power TC-ResNet AI Accelerator for Efficient Keyword Spotting by Paul Palomero Bernardo, Christoph Gerum, Adrian Frischknecht, Konstantin Lübeck, and Oliver Bringmann, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 39, Issue: 11, Nov. 2020, https://doi.org/10.1109/TCAD.2020.3012320.

Von TUK wurden vier Vortragsbeiträge zum Intel internen SCAP Workshop 2020 (virtuell) eingeladen und geleistet, 28.9.-1.10.2020.

Pressemitteilung IFX, am 24. September 2020 „Projekt Scale4Edge startet im Rahmen der Leitinitiative „Vertrauenswürdige Elektronik“ des Bundesforschungsministeriums - Skalierbares Ökosystem für Spezialprozessoren für das Internet der Dinge wird angestrebt“ (https://www.infineon.com/cms/de/about-infineon/press/press-releases/2020... [14])

W. Ecker: ZuSE Workshop am 22.9.2020

Best Paper Award: "Efficient Cross-Level Testing for Processor Verification: A RISC-V Case-Study", Vladimir Herdt, Daniel Große, Universität Bremen, DE, Eyck Jentzsch, MINRES Technologies GmbH, DE, Rolf Drechsler, Universität Bremen, DE, FDL 2020, September 2020

W. Ecker: Silicon Saxony: Vortrag am 11.9.2020

Vladimir Herdt, Daniel Große, Jonas Wloka, Tim Güneysu, and Rolf Drechsler. 2020. Verification of Embedded Binaries using Coverage-guided Fuzzing with SystemC-based Virtual Prototypes. In Proceedings of the 2020 on Great Lakes Symposium on VLSI (GLSVLSI '20). Association for Computing Machinery, New York, NY, USA, 101–106. https://doi.org/10.1145/3386263.3406899

Pressemitteilung OSS mit TUK, RB und MNRS, im September 2020

Pressemeldung der TU Kaiserslautern am 6.7.2020

W. Ecker: Pressekonferenz „Vertrauenswürdige Elektronik“ am 9.6.2020

HNI Newsletter Ausgabe 01 2020 der Universität Paderborn „Neues Verbundprojekt Scale4Edge“. S.8: https://www.hni.uni-paderborn.de/fileadmin/Publikationen/hni_aktuell/hni_aktuell_1_2020.pdf

muRISCV-NN Präsentation in RISC-V SIG für Graphics&ML

Das CHIPS-Framework ist eine in Scala eingebettete domänenspezifische Sprache (DSL), die die Spezifikation von leichtgewichtigen Verifikationseigenschaften auf verschiedenen Abstraktionsebenen unter Verwendung des assertion-basierten Verifikationsparadigmas ermöglicht; Open Source; https://github.com/fzi-forschungszentrum-informatik/chips-core

Rust-Bibliothek, welche eine FIRRTL-AST-Darstellung und zugehörige Managementschnittstellen, einschließlich eines Parsers und Formatierers, bereitgestellt; Open Source; https://github.com/fzi-forschungszentrum-informatik/firrtl-ast

Erweiterung des Rocket Chip Generator zur Bereitstellung von Informationen zum Register-Mapping. Diese Erweiterung ist zur Nutzung der HW/SW-Co-Verifikation notwendig. Im Rahmen der Erweiterung wurden Änderungen zur Vereinfachung des Wechsels auf Scala3 eingepflegt; Open Source; https://github.com/chipsalliance/rocket-chip

Das Projekt Scale4Edge wird unter den Förderkennzeichen 16ME0122K-140, 16ME0465, 16ME0900, 16ME0901 im Förderprogramm ZuSE durch das deutsche Bundesministerium für Bildung und Forschung (BMBF) gefördert.

Links:
[1] https://doi.org/10.1109/TCAD.2024.3445810;
[2] https://dx.doi.org/10.1561/3500000003;
[3] https://www.asplos-conference.org/asplos2024/
[4] https://date24.date-conference.com/programme
[5] https://edas.info/p29519#S1569607348;
[6] https://www.intel.com/content/www/us/en/security/security-practices/security-research/hardware-security-academic-award.html
[7] https://doi.org/10.1109/DAC18074.2021.9586248;
[8] https://doi.org/10.1007/978-3-031-15074-6_16
[9] https://doi.org/10.1007/s11432-020-3308-4
[10] https://www.tinyml.org/event/emea-2021/
[11] https://riscvforumdttc2021.sched.com/event/jGkT
[12] https://cps-vo.org/group/DESTION2021/program;
[13] https://github.com/fzi-forschungszentrum-informatik/chips-core

[14] https://www.infineon.com/cms/de/about-infineon/press/press-releases/2020/INFXX202009-090.html