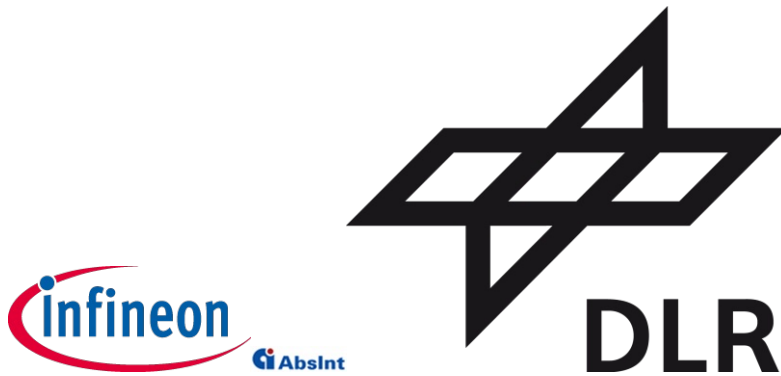


Success Story: Multi-Compiler Support

2023/11/06



Introduction

The Scale4Edge project aims to create an efficient RISC-V ecosystem for edge application optimization. It focuses on developing a versatile platform to provide cost-effective, application-specific edge devices and services for various market segments. This is achieved through fine-grained adaptation of generic components, covering CPU instructions, user/application software, and operating system/firmware levels. The ecosystem is highly scalable and customizable to individual applications, supporting various hardware architectures and non-functional properties like energy efficiency, fault tolerance, reliability, safety, and security.

The Scale4Edge ecosystem currently contains three different compilers, addressing different use-cases of the ecosystem:

CompCert is a formally verified compiler for safety relevant application of high assurance levels

X-LLVM is an extendible compiler for custom instructions based on Clang/LLVM

A custom configurable GCC compiler

CompCert - a Verified Compiler

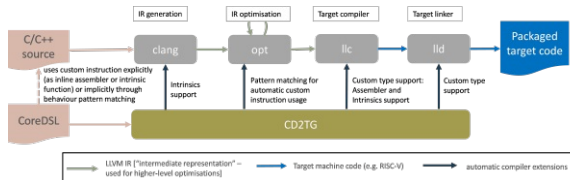
CompCert is a compiler for the C programming language (<https://www.absint.com/compcert/>). It accepts most of the ISO-C 99 language, with some minor exceptions and a few useful extensions. Its intended use is the compilation of life-critical and mission-critical software written in C and meeting high levels of assurance.

What sets CompCert apart from any other production compiler is that it is formally verified, using machine-assisted mathematical proofs, to be exempt from miscompilation issues. In other words, the executable code it produces is proved to behave exactly as specified by the semantics of the source C program. This level of confidence in the correctness of the compilation process contributes to meeting the highest levels of software assurance. Using the CompCert C compiler is a natural complement to applying formal verification techniques (static analysis, program proof, model checking) at the source code level: the correctness proof of CompCert guarantees that all safety properties verified on the source code automatically hold as well for the generated executable.

In 2022, the Association for Computing Machinery, ACM, presented the CompCert development team with the prestigious ACM Software System Award (<https://www.absint.com/releases/220511.htm>) and the ACM SIGPLAN Programming Languages Software Award (<https://www.sigplan.org/Awards/Software/>).

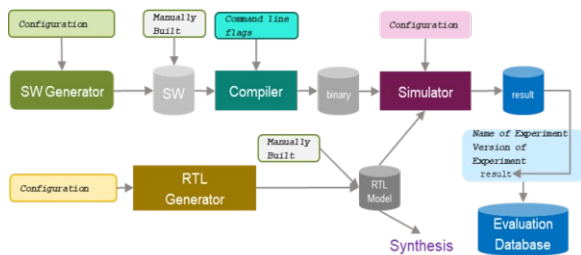
During the Scale4Edge project, CompCert was given a backend for RISC-V. CompCert for RISC-V generates code for the base instruction sets RV32I and RV64I with standard extensions M (Integer Multiplication and Division), F (Single-Precision Floating-Point), and D (Double-Precision Floating-Point). CompCert for RISC-V has been combined with picolibc (<https://github.com/picolibc/picolibc>), a C library designed for embedded 32- and 64-bit microcontrollers with small memory. After some changes proposed by the CompCert developers (mostly to avoid GCC/Clang specific language extensions), the picolibc source code can now be compiled with CompCert.

X-LLVM - an extendible Compiler for custom instructions



Existing toolchains with RISC-V support cannot yet be flexibly extended to quickly support ISA extensions. In addition, RISC-V extensions in the Scale4Edge project are described using a separate language called CoreDSL. An automated translation of these CoreDSL definitions into corresponding toolchain extensions, as far as possible, is therefore not only desirable for reasons of flexibility, but also almost inevitable for reasons of consistency. For this reason, the described hardware (processor core) and a virtual platform and a compiler with support of custom defined instructions can be generated from CoreDSL. We have successfully automated the modification of Clang/LLVM to support custom instructions throughout the whole software toolchain (compiler, linker debugger), as depicted in the figure. Based on a CoreDSL description of the custom instructions, the extendible compiler toolchain (called X-LLVM) implements a compiler generator (called CD2TG) to provide the defined custom instructions as assembler code or intrinsic function for explicit usage. If possible, custom instructions are also implicitly used by the compiler (e.g., MAC (Multiply Accumulate) or Zero Overhead Loop). If this were done based on a manual translation, there would be a potential for an incorrect or at least inconsistent translation at each individual step. By automating this process, these errors can be avoided. Another benefit of automation is the speed with which the different artifacts can be regenerated. For example, if a new CoreDSL description is created or an existing description is revised, the corresponding tool chains can be triggered directly to generate the different artifacts and thus be able to test the newly defined instructions directly and revise them further if necessary. The current open source release of X-LLVM is available at <https://github.com/DLR-SE/extendible-compiler>.

GCC - the power of optimization



gcc supports plenty of optimization opportunities, most can be controlled by over 120 command line flags.

The Infineon RISC-V RTL generator supports also plenty of configurations (superset of CoreDSL) to generate a huge number of RISC-V variants differing in function, performance in clock cycles and performance in clock period. From the perspective of compiler performance analysis, the number of clock cycles is relevant. The maximum clock period is provided by the synthesis - or better R2G - flow. Performance evaluation is done by RTL simulation but can be moved to FPGAs and Emulation as RISC-V or SoC features (Timers) are used to measure time. For evaluation, classical benchmarks but also generated software has been applied. Of course, the framework is also used to run regression over the complete generation chain and validate the compiler result for a specific code and application.

Results worth mentioning are a substantial impact of compiler optimization, more performance when comparing to other non-RISC-V cores but also a non-neglectable memory footprint overhead.

Contact:

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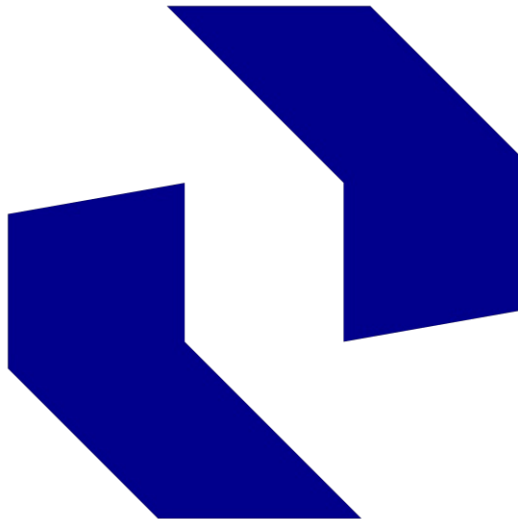
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Herunterladen:
 Success Story: Multi-Compiler Support



For a commercially successful development of edge devices for a wide range of applications, a whole ecosystem of tools and hardware components is mandatory. Ensuring the safe, secure, and reliable design and operation of these devices is an indispensable, but challenging requirement for many of these applications. The Scale4Edge project aims to address this challenge by enabling a comprehensive RISC-V-based ecosystem that helps ensure the correct and secure functioning throughout the whole design process and lifetime of an edge system: The ecosystem encompasses tools for functional verification—both using virtual prototypes in an early stage of development and using formal methods—, security verification, software-based self-test (SBST), and system visualization and debugging. With the development of this hardware verification and validation ecosystem, the Scale4Edge project aims to create optimized and reliable edge devices that meet the high demands of modern industries.

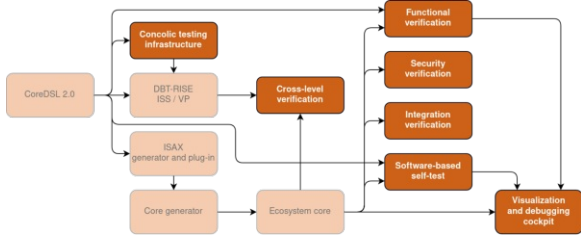


Figure 1: The Scale4Edge Hardware Verification Ecosystem

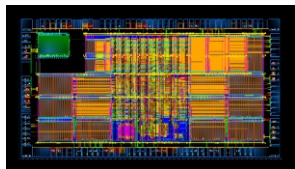
The Scale4Edge project has made significant strides in hardware verification and validation for RISC-V platforms, with multiple partners contributing to its success. The components of the hardware verification ecosystem are shown in Figure 1. The **University of Bremen** developed a comprehensive cross-level verification approach and a concolic testing infrastructure. **Siemens EDA**—an associated partner—created new functional verification tools for processor verification while the **University of Kaiserslautern-Landau (RPTU)** focused on formal security analysis with Unique Program Execution Checking (UPEC). The **FZI Research Center for Information Technology (FZI)** devised methods for specifying, generating, and verifying hardware properties in System-on-Chip (SoC) platforms, with the **University of Freiburg** and **Concept Engineering** contributing to in-field monitoring and testing (SBST) as well as debugging and visualization tooling. The collaborative efforts of the project partners around the Scale4Edge ecosystem core, developed by **MINRES** according to the ISO 26262 safety standard, resulted in a comprehensive hardware verification and validation flow with award winning methods and industry-proven EDA tools.

Herunterladen:

[Success Story: The Scale4Edge Hardware Verification and Validation Ecosystem for RISC-V Platforms](#)

Success Story: Software-driven CPU implementation

2022/11/28



Many application domains including automotive, industry automation, IoT, and space, require the usage of well-tailored edge devices capable of processing data from various sensor sources using AI, DSP, and classical software algorithms. Data processing at edge devices must satisfy real-time requirements while consuming as little electric energy and memory footprint as possible. Moreover, for many applications, the aspects of safety, security, and reliability are equally important as performance or electric energy consumption. Therefore, application-specific system-on-chip architectures for edge devices require high customization in terms of the most appropriate performance class of the processor core including necessary custom processor extensions, the memory architecture and capacity, and the design of a parameterizable AI accelerator architecture. The BMBF project Scale4Edge aims at enabling a comprehensive RISC-V-based ecosystem to efficiently assemble optimized edge devices.

By using the Scale4Edge ecosystem, the project partner Bosch developed a neural-network based audio event detection model. This use-case has been ported to a Pulpissimo-based SoC platform[1] using components and software of the Scale4Edge ecosystem.

Herunterladen:

[Scale4Edge Success Story: Software-driven CPU implementation](#)

Scale4Edge @ 2022 IEEE 35th International System-on-Chip Conference (SOCC)

2022/08/19

Monday, September 5, 2022 14:05 - 15:25 (Europe/London)

Industrial Session: RISC-V: Evolution, Innovation and Research Challenges of Open-ISA

Room: Britannic Suite

Abstract

Standards are known to slow down research and innovation in their area. Therefore, one might fear that the RISC-V ISA, as a standard, slows down processor and ISA development.

Bringing TinyML to RISC-V With Specialized Kernels and a Static Code Generator Approach

2022/06/21

@embedded world 2022, 21.6.2022 11:00: <https://www.embedded-world.de/en/conferences-programme/programme-overvie...>

Rafael Stahl (Technical University of Munich)

PROJEKT: RISC-V-PROZESSOREN VERTRAUENSWÜRDIG MACHEN

2021/11/14

Untertitel:

Im Rahmen der Leitinitiative „Vertrauenswürdige Elektronik“ ist das Forschungsprojekt „Scale4Edge“ an den Start gegangen. 22 Partner aus Wissenschaft und Wirtschaft bündeln darin ihre Kompetenzen, um den Einsatz von vertrauenswürdigen Spezialprozessoren rund um die Open-Source-Architektur RISC-V voranzutreiben.

Publishing Date: Mo., 2020/09/28

Found at: E&E Entwicklung Elektronik

Found at: PROJEKT: RISC-V-PROZESSOREN VERTRAUENSWÜRDIG MACHEN

Die Entwicklung und den Einsatz von vertrauenswürdigen Spezialprozessoren in Deutschland vorantreiben – so lautet das Ziel von „Scale4Edge“. Unter der Koordination von Infineon nehmen sich insgesamt 22 Projektpartner dieser Aufgabe in den kommenden drei Jahren an. Erste Ergebnisse werden bereits Ende 2020 erwartet.

Exploring Static Code Generation and SIMD-Acceleration for Machine Learning on RISC-V by Rafael Stahl, Technical University of Munich @RISC-V Forum on "Developer Tools & Tool Chains" on June 2, 2021 18:05 CEST

2021/05/14

The deployment of machine learning applications on microcontrollers known as TinyML enables new low-power applications and always-on devices. The RISC-V architecture is attractive for such microcontrollers, because it provides easy extensibility, a healthy ecosystem and no license costs. The major challenges with resource-constrained devices are run time and memory usage. Existing machine learning frameworks provide runtime libraries that dynamically load and execute a model, but this entails overheads.

RISC-V Summit 2020: Tutorial with OpenHW and Silicon Labs

2021/05/04

RISC-V Tutorial Video

Tutorial session from RISC-V Summit 2020 with OpenHW and Silicon Labs.

Watch the full video featuring Scale4Edge partner OneSpin's Design Verification Product Manager Sven Beyer & OpenHW's Mike Thompson.



Scale4Edge Partner MINRES @ Accellera's SystemC Evolution Fika

2021/03/16

March 17, 2021
16:00 - 18:00 CET
Virtual event

Accellera's SystemC Evolution events are expanding with the addition of SystemC Evolution Fikas! Fika is a tradition of sharing a coffee, slowing down a bit, and talking about things that we care about.

The first SystemC Evolution Fika will take place on March 17 from 16:00 to 18:00 CET. It will be free of charge and virtual. There are two presentations planned: one on SystemC and Python and one about the Intel SystemC Compiler.

Scale4Edge Projektpartner TU Dresden gewinnt den Pilotinnovationswettbewerb "Energieeffizientes KI-System"

2021/03/15

Wir gratulieren unserem Scale4Edge Projektpartner Christian Mayr und sein Team von der TU Dresden zum Gewinn des Pilotinnovationswettbewerb "Energieeffizientes KI-System" in der Gruppe der 22nm Designs. Das Team der TU Dresden hat sich mit einer sehr guten Lösung gegen eine starke Konkurrenz durchgesetzt.

[« erste Seite](#) [« vorherige Seite](#) [1](#) [2](#) [3](#) [4](#) [nächste Seite](#) [» letzte Seite](#) »

Das Projekt Scale4Edge wird unter den Förderkennzeichen 16ME0122K-140, 16ME0465, 16ME0900, 16ME0901 im Förderprogramm ZuSE durch das deutsche Bundesministerium für Forschung, Technologie und Raumfahrt (BMFTR) gefördert.

Quell-URL: <https://project.edacentrum.de/scale4edge/node>