Success Story: The Scale4Edge Hardware Verification and Validation Ecosystem for RISC-V Platforms

2023/05/05

For a commercially successful development of edge devices for a wide range of applications, a whole ecosystem of tools and hardware components is mandatory. Ensuring the safe, secure, and reliable design and operation of these devices is an indispensable, but challenging requirement for many of these applications. The Scale4Edge project aims to address this challenge by enabling a comprehensive RISC-V-based ecosystem that helps ensure the correct and secure functioning throughout the whole design process and lifetime of an edge system: The ecosystem encompasses tools for functional verification—both using virtual prototypes in an early stage of development and using formal methods—, security verification, software-based self-test (SBST), and system visualization and debugging. With the development of this hardware verification and validation ecosystem, the Scale4Edge project aims to create optimized and reliable edge devices that meet the high demands of modern industries.

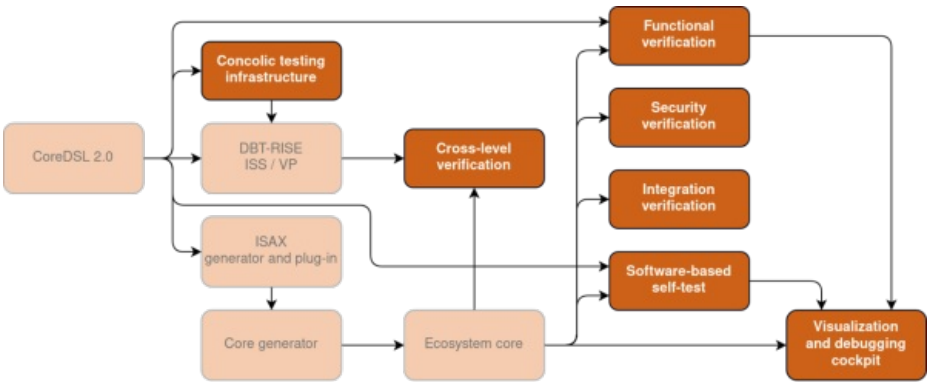


Figure 1: The Scale4Edge Hardware Verification Ecosystem

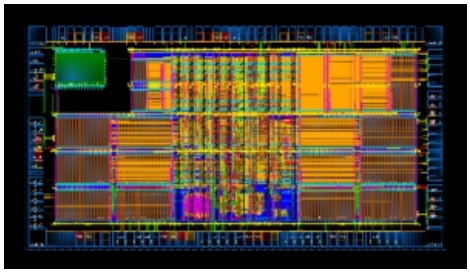
The Scale4Edge project has made significant strides in hardware verification and validation for RISC-V platforms, with multiple partners contributing to its success. The components of the hardware verification ecosystem are shown in Figure 1. The **University of Bremen** developed a comprehensive cross-level verification approach and a concolic testing infrastructure. **Siemens EDA**—an associated partner—created new functional verification tools for processor verification while the **University of Kaiserslautern-Landau** (*RPTU)* focused on formal security analysis with Unique Program Execution Checking (UPEC). The **FZI Research Center for Information Technology** (FZI) devised methods for specifying, generating, and verifying hardware properties in System-on-Chip (SoC) platforms, with the **University of Freiburg** and **Concept Engineering** contributing to in-field monitoring and testing (SBST) as well as debugging and visualization tooling. The collaborative efforts of the project partners around the Scale4Edge ecosystem core, developed by **MINRES** according to the ISO 26262 safety standard, resulted in a comprehensive hardware verification and validation flow with award winning methods and industry-proven EDA tools.

Herunterladen:

Success Story: The Scale4Edge Hardware Verification and Validation Ecosystem for RISC-V Platforms

Success Story: Software-driven CPU implementation

2022/11/28



Many application domains including automotive, industry automation, IoT, and space, require the usage of well-tailored edge devices capable of processing data from various sensor sources using AI, DSP, and classical software algorithms. Data

processing at edge devices must satisfy real-time requirements while consuming as little electric energy and memory footprint as possible. Moreover, for many applications, the aspects of safety, security, and reliability are equally important as performance or electric energy consumption. Therefore, application-specific system-on-chip architectures for edge devices require high customization in terms of the most appropriate performance class of the processor core including necessary custom processor extensions, the memory architecture and capacity, and the design of a parameterizable AI accelerator architecture. The BMBF project Scale4Edge aims at enabling a comprehensive RISC-V-based ecosystem to efficiently assemble optimized edge devices.

By using the Scale4Edge ecosystem, the project partner Bosch developed a neural-network based audio event detection model. This use-case has been ported to a Pulpissimo-based SoC platform[1] using components and software of the Scale4Edge ecosystem.

Herunterladen:
Scale4Edge Success Story: Software-driven CPU implementation

Scale4Edge @ 2022 IEEE 35th International System-on-Chip Conference (SOCC)

2022/08/19

Monday, September 5, 2022 14:05 - 15:25 (Europe/London)

Industrial Sesson: RISC-V: Evolution, Innovation and Research Challenges of Open-ISA

Room: Britannic Suite

Abstract

Standards are known to slow down research and innovation in their area. Therefore, one might fear that the RISC-V ISA, as a standard, slows down processor and ISA development.

Bringing TinyML to RISC-V With Specialized Kernels and a Static Code Generator Approach

2022/06/21

@embedded world 2022, 21.6.2022 11:00: https://www.embedded-world.de/en/conferences-programme/programme-overvie...

Rafael Stahl (Technical University of Munich)

PROJEKT: RISC-V-PROZESSOREN VERTRAUENSWÜRDIG MACHEN

2021/11/14

... in the Press

Untertitel:
Im Rahmen der Leitinitiative „Vertrauenswürdige Elektronik“ ist das Forschungsprojekt „Scale4Edge“ an den Start gegangen. 22 Partner aus Wissenschaft und Wirtschaft bündeln darin ihre Kompetenzen, um den Einsatz von vertrauenswürdigen Spezialprozessoren rund um die Open-Source-Architektur RISC-V voranzutreiben.

Publishing Date: Mo., 2020/09/28
Found at: E&E Entwicklung Elektronik
Found at: PROJEKT: RISC-V-PROZESSOREN VERTRAUENSWÜRDIG MACHEN

Die Entwicklung und den Einsatz von vertrauenswürdigen Spezialprozessoren in Deutschland vorantreiben – so lautet das Ziel von „Scale4Edge“. Unter der Koordination von Infineon nehmen sich insgesamt 22 Projektpartner dieser Aufgabe in den kommenden drei Jahren an. Erste Ergebnisse werden bereits Ende 2020 erwartet.

Exploring Static Code Generation and SIMD-Acceleration for Machine Learning on RISC-V by Rafael Stahl, Technical University of Munich @RISC-V Forum on "Developer Tools & Tool Chains" on June 2, 2021 18:05 CEST

2021/05/14

The deployment of machine learning applications on microcontrollers known as TinyML enables new low-power applications and always-on devices. The RISC-V architecture is attractive for such microcontrollers, because it provides easy extensibility, a healthy ecosystem and no license costs. The major challenges with resource-constrained devices are run time and memory usage. Existing machine learning frameworks provide runtime libraries that dynamically load and execute a model, but this entails overheads.

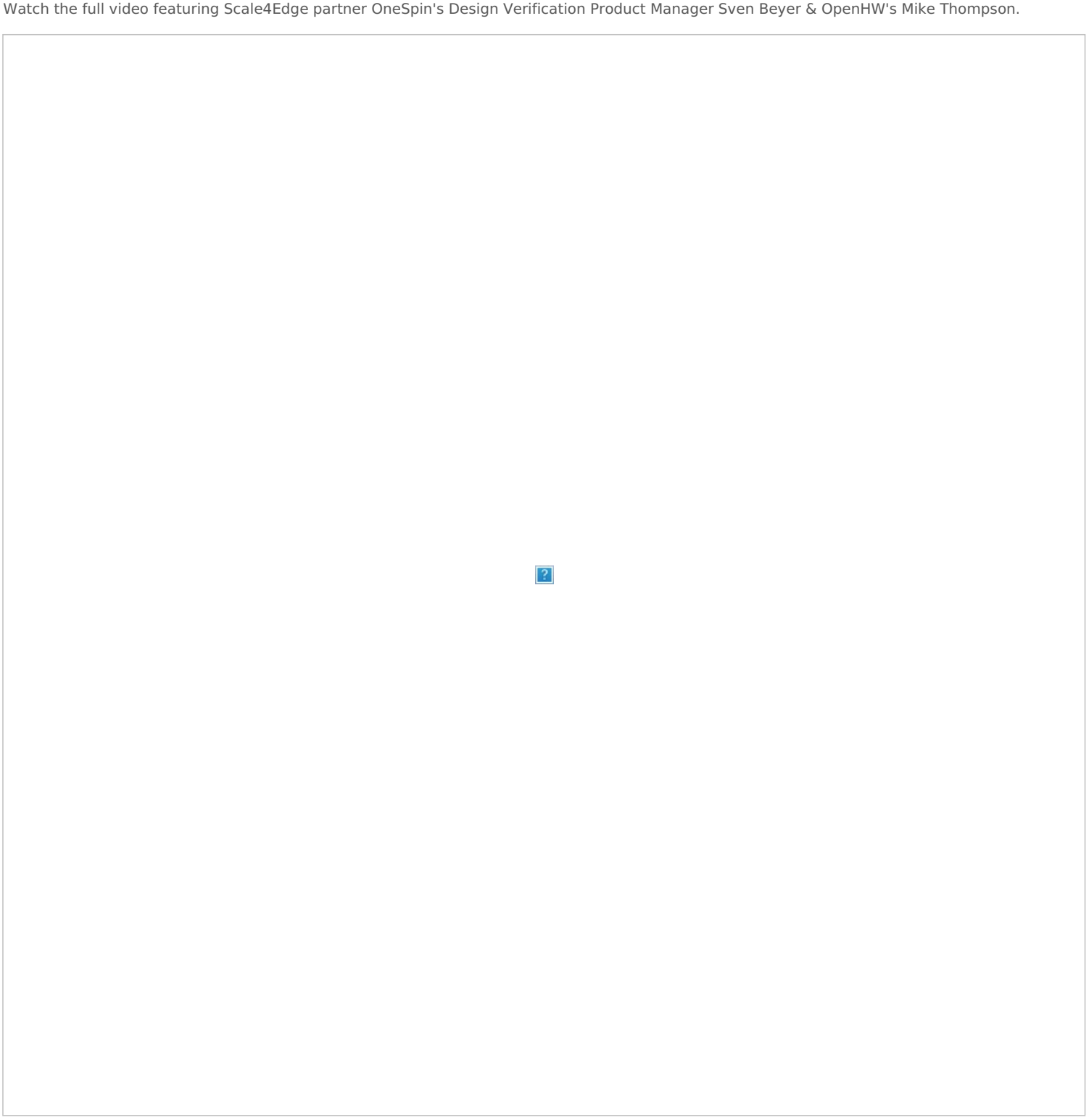
RISC-V Summit 2020: Tutorial with OpenHW and Silicon Labs

2021/05/04

RISC-V Tutorial Video

Tutorial session from RISC-V Summit 2020 with OpenHW and Silicon Labs.

Watch the full video featuring Scale4Edge partner OneSpin's Design Verification Product Manager Sven Beyer & OpenHW's Mike Thompson.



Scale4Edge Partner MINRES @ Accellera's SystemC Evolution Fika

2021/03/16

March 17, 2021
16:00 - 18:00 CET
Virtual event

Accellera's SystemC Evolution events are expanding with the addition of SystemC Evolution Fikas! Fika is a tradition of sharing a coffee, slowing down a bit, and talking about things that we care about.

The first SystemC Evolution Fika will take place on March 17 from 16:00 to 18:00 CET. It will be free of charge and virtual. There are two presentations planned: one on SystemC and Python and one about the Intel SystemC Compiler.

Scale4Edge Projektpartner TU Dresden gewinnt den Pilotinnovationswettbewerb "Energieeffizientes KI-System"

2021/03/15

Wir gratulieren unserem Scale4Edge Projektpartner Christian Mayr und sein Team von der TU Dresden zum Gewinn des Pilotinnovationswettbewerb

"Energieeffizientes KI-System" in der Gruppe der 22nm Designs. Das Team der TU Dresden hat sich mit einer sehr guten Lösung gegen eine starke Konkurrenz durchgesetzt.

Join Scale4Edge Session on April 28, 2021 20:15 CET

2021/02/25

Embedded IoT World

April 28 - 29, 2021

Virtual Event

Scale4Edge is revolutionizing the way edge computing devices and applications are developed - aiming to increase performance, safety, and security.

Backed by the German Ministry of Education and Research, this research project is building an ecosystem for scalable edge computing based on RISC-V architecture.

On April 28, join Embedded IoT World Scale4Edge sessions to learn:

How "virtual prototyping first" speeds up and improves quality for scalable RISC-V based design

How to use the VP-VIBES framework to quickly bring virtual prototypes into your design flows

How to integrate DNN accelerators to bring more processing power and intelligence close to the sensor

CHOOSE MY PASS TO ATTEND

JOIN SCALE4EDGE SESSIONS ON APRIL 28:

Virtual System Prototypes: Enabling an Application-Driven Hardware Design Flow

Vladimir Herdt

Senior Researcher, University of Bremen / DFKI

VIEW SESSION DETAILS >>

Advanced Virtual Prototyping: Modeling, Simulation and Verification

VIEW SESSION DETAILS >>

Designing Application-Specific DNN Accelerators for RISC-V Based Edge AI Platforms

Christian Mayr

Professor, Technische Universität Dresden

VIEW SESSION DETAILS >>

REGISTER TO JOIN THESE SESSIONS

All Access and Premium Passes include access to join these sessions.

Das Projekt Scale4Edge wird unter den Förderkennzeichen 16ME0122K-140, 16ME0465, 16ME0900, 16ME0901 im Förderprogramm ZuSE durch das deutsche Bundesministerium für Forschung, Technologie und Raumfahrt (BMFTR) gefördert.
