IP²

Configurable System-on-Chip: Coarse-grain XPP-based Architecture

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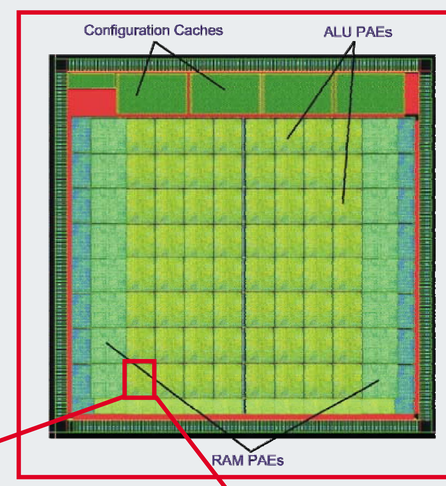
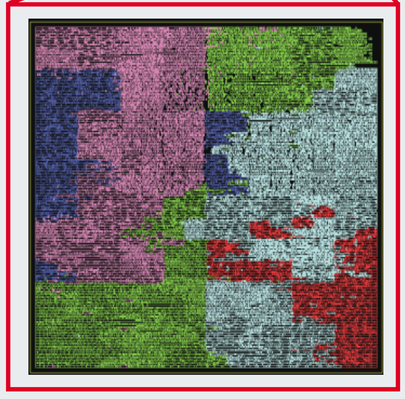
8x8 XPP Array layout, synthesised in UMC 0.13 µm technology



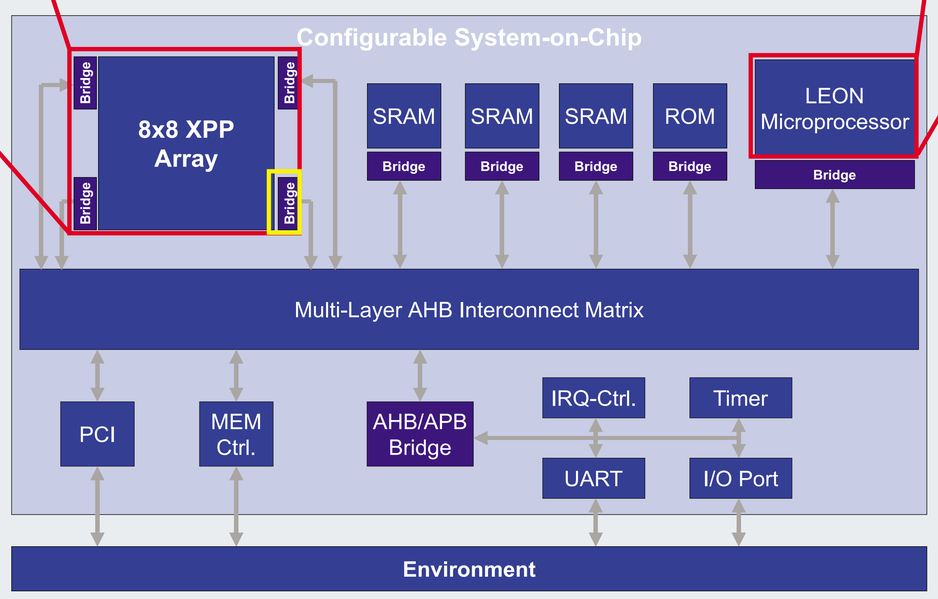


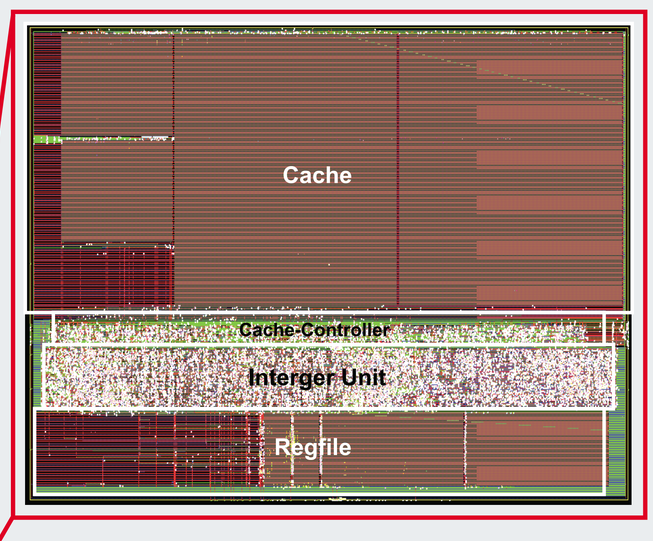
Legend:
- ALU_OBJECT
- BREG_OBJECT
- FREG_OBJECT
- SWITCH_OBJECT
- SWITCH_OBJECTs450
- CM_SEGMENT_INTERFACE

Single ALU-PAE layout: semi-hierarchical standard cell synthesis (UMC 0.13 µm CMOS technology)

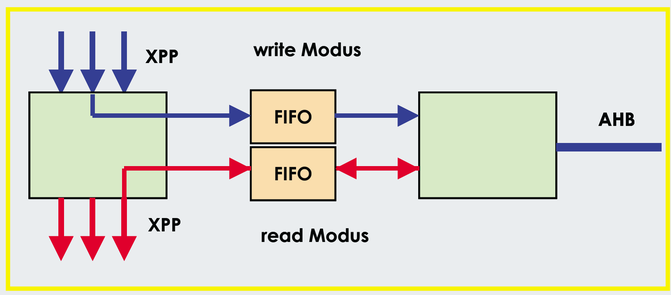
CSoC - Components

- 8x8 XPP array
- Leon RISC microprocessor
- on-chip SRAM/ROM modules
- external memory controler
- multi-layer AHB Interconnect matrix
- IRQ-controler, UARTS, Timer, I/O ports





Leon Microprocessor layout, synthesised in UMC 0.13 µm technology



XPP2AHB Master/Slave Bridge

XPP-/LEON-based CSoC Architecture

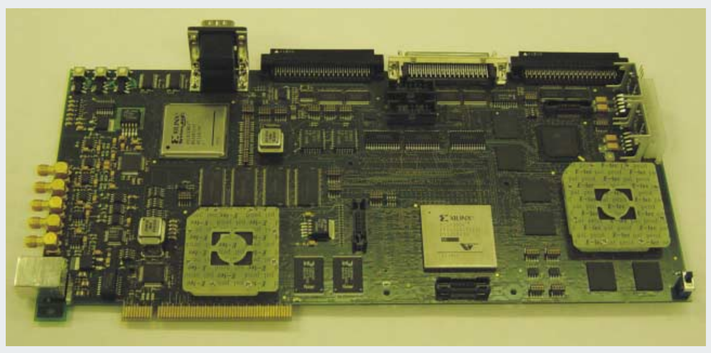
LEON Microprocessor

- available as a **free IP** Core from ESA (European Space Agency)
- **synthesisable VHDL model** of a 32-bit processor with an instruction set according to the IEEE-1754
- LEON integer unit (IU) implements SPARC integer instructions as defined in SPARC Architecture Manual version 8
- **5-stage instruction pipeline**

LEON Synthesis Results (2x8KB Caches)

- approx. 15.000 standard cells
- 0,9 mm² area requirements
- clock frequency up to 250 Mhz

XPP64A Development Platform



XPP - eXtreme Processing Platform

- Hierarchical array of coarse-grain Processing Array Elements (PAEs)
- powerful run-time reconfiguration mechanism
- main distinguishing features:
  - automatic packet-handling mechanism
  - sophisticated hierarchical Configuration protocols

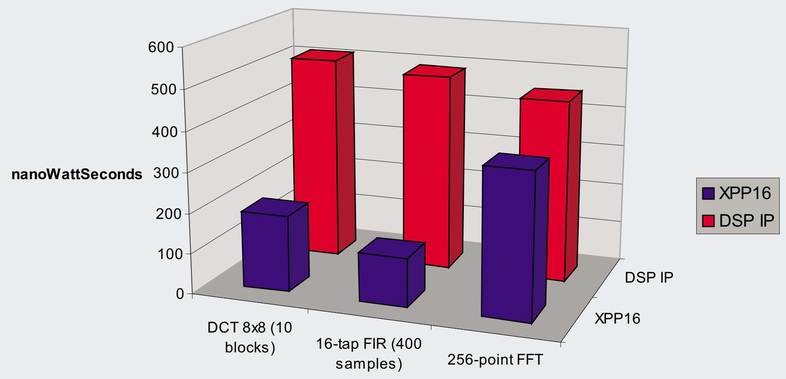
XPP Application Results Example

- **MPEG-4:**
  - 3 different frame types
- **iDCT:** 40 operations onto **4x4 XPP** array
  - 74 clock cycles for decoding of a single 8x8 pixel block
- **PAL image:**
  - 720x576 pixel x 24bit = 1,2 MB/frame
  - 25 frames/sec => 30 MB/s
  - 6480 blocks => 479.520 cycles/frame
  - 25 frames/s => 11.988.000 cycles/s

XPP Energy Consumtion

CMOS, 0.13µm, 100 Mhz

Algorithm	XPP16	DSP IP
MPEG Video 2D DCT (8x8)	19 nWattSeconds	51 nWattSeconds
Real 16 Tap FIR Filter (40 Samples)	12 nWattSeconds	49 nWattSeconds
256-point FFT	360 nWattSeconds	453 nWattSeconds



Multi-layer AHB

- routes **multiple transfers** at the same time from masters to addressed slaves
- model is **highly parametrizable** with regards to AHB module count, AHB width, address spaces, etc.
- parallel transfers boost the maximum bus performance to a multiple of standard AHB performance