# Publications

2025/08/01

Unifying IP Specification Through Formal Hardware Function Sets: An Industrial Case Study, Robert Kunzelmann, Infineon Technologies AG and Technical University of Munich, DE <robertniklas [dot] kunzelmann@infineon [dot] com>, Maximilian Berger, Infineon Technologies AG, DE and and Technical University of Munich, DE, Vinod Bangalore Ganesh, Infineon Technologies AG, DE and and Technical University of Dresden, DE, Rachana R. Pai, Infineon Technologies AG, DE, Wolfgang Ecker, Infineon Technologies AG and Technical University of Munich, DE, IEEE MCSoC, 15.12.2025, Singapore, SG.

Leveraging Model-Driven Architecture for Efficient Custom Instruction Utilization in Embedded Systems in C and Rust, Raphael Kunz, Infineon Technologies AG and Technical University of Munich, DE <raphael [dot] kunz@infineon [dot] com>, Mayuri.Bhadra <mayuri [dot] bhadra12@ gmail [dot] com>, Chen Lijun, Infineon Technologies AG and Technical University of Munich, DE <Lijun [dot] Chen@infineon [dot] com>, Stephanie Ecker, Chipglobe GmbH and Infineon Technologies AG, DE <Ecker [dot] external2@infineon [dot] com>, Wolfgang Ecker, Infineon Technologies AG and Technical University of Munich, DE, FDL, 10.09.2025, St. Goar, DE.

FastPath: A Hybrid Approach for Efficient Hardware Security Verification, Lucas Deutschmann1, Andres Meza2, Dominik Stoffel1, Wolfgang Kunz1, and Ryan Kastner2; 1RPTU Kaiserslautern-Landau, 2UC San Diego; 62th IEEE/ICM Design Automation Conference (DAC), San Francisco, USA, 2025.

„Embench™ IOT 2.0 and DSP 1.0: Modern Embedded Computing Benchmarks“ David Patterson et. al. (Co-Autoren sind Konrad Moron und Stefan Wallentowitz von der Hochschule München) erscheint in IEEE Computer 2025

Benchmarking TinyML CNN Kernels on RVV 1.0 Hardware: GCC 14 vs. LLVM 19, Philipp van Kempen, Benedikt Witteler, Ulf Schlichtmann (TUM), Daniel Mueller-Gritschneder (TUW), Extended Abstract, RISC-V Summit Europe 2025, 12.-15.5.2025, Paris

Benchmarking TinyML CNN Kernels on RVV 1.0 Hardware: GCC 14 vs. LLVM 19, Philipp van Kempen, Benedikt Witteler, Ulf Schlichtmann (TUM), Daniel Mueller-Gritschneder (TUW), Poster, RISC-V Summit Europe 2025, 12.-15.5.2025, Paris

Tracing-Bibliothek nach der ETrace-Spezifikation (https://github.com/riscv-non-isa/riscv-trace-spec/ [1]), FZI

LLM-assisted Methodology for Embedded Software Performance Estimation on RISC-V, Weiyan Zhang <weiyan@uni-bremen [dot] de> (1) , Muhammad Hassan (1,2) , and Rolf Drechsler (1,2), (1) Institute of Computer Science, University of Bremen, Germany, (2) Cyber-Physical Systems, DFKI GmbH, Bremen, Germany, RISC-V Summit Europe 2025, 12.05.2025 - 15.05.2025, Paris, FR.

CrosSym: Cross-Level Verification of SystemC Peripherals using Symbolic Execution, Karl Aaron Rudkowski <karlaaron@uni-bremen [dot] de> (1) , Sallar Ahmadi-Pour (1) , and Rolf Drechsler (1,2), (1) Institute of Computer Science, University of Bremen, Germany, (2) Cyber-Physical Systems, DFKI GmbH, Bremen, Germany, DDECS 2025, 05.05.2025 - 07.05.2025, Lyon, FR.

LLM-assisted Performance Estimation of Embedded Software on RISC-V Processors, Weiyan Zhang <weiyan@uni-bremen [dot] de> (1) , Muhammad Hassan (1,2) , and Rolf Drechsler (1,2), (1) Institute of Computer Science, University of Bremen, Germany, (2) Cyber-Physical Systems, DFKI GmbH, Bremen, Germany, DDECS 2025, 05.05.2025 - 07.05.2025, Lyon, FR.

On April 4 2025, EPoSS and INSIDE industry associations hosted a webinar outlining Europe’s strategic direction in Edge AI, a domain at the forefront of AI innovation.

These are the key takeaways:

Cooperation before competition: European tech leaders emphasized the need for a united front to build competitive ecosystems.
Edge AI is accelerating: From LLMs to digital twins and frugal AI, innovation is rapidly reshaping the edge computing stack.
Cross-layer optimization is crucial: True impact requires co-design across chips, software, and applications.
Europe must act now: Limited access to advanced nodes and reliance on non-EU infrastructure highlight the urgency for investment and collaboration.

A call to action: The Edge AI Working Group is advocating for a European roadmap, open ecosystems, and robust training infrastructure. Short reports on all parts of the workshop are now available for download. Our special thanks go all contributors and presenters:

Inessa Seifert, VDI/VDE-IT
Paolo Azzoni, INSIDE
Danilo Pau, STMicroelectronics
Anders Lindgren, RISE
Alain Pagani, German Research Center for Artificial Intelligence (DFKI)
Hans-Jörg Vögel, BMW
Lior Klein, MultiSpin.AI
Davis Sawyer, NXP
Wolfgang Ecker, Infineon
Downloads: https://www.smart-systems-integration.org/publication/future-edge-ai-notes-workshop

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Paul Palomero Bernardo, Patrick Schmid, Christoph Gerum, and Oliver Bringmann. 2025. Compiler-aware AI Hardware Design for Edge Devices. In The 8th International Workshop on Edge Systems, Analytics and Networking (EdgeSys '25), March 30-April 3, 2025, Rotterdam, Netherlands. ACM, New York, NY, USA, 6 pages. https://doi.org/10.1145/3721888.3722095

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A Hardware-assisted Approach for Non-invasive and Fine-grained Memory Power Management in MCUs, Michael Kuhn, Patrick Schmid and Oliver Bringmann, Embedded Systems, University of Tübingen, Germany, DATE 2025, 31.3-2.4.2025, Lyon, France.

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Towards Non-Intrusive SystemC Checkpointing for Digital Virtual Prototypes, Deepak Ravibabu (1), Muhammad Hassan <hassan@uni-bremen [dot] de> (1,3), Thilo Vörtler (2), Karsten Einwich (2), Rolf Drechsler (1,3), and Daniel Große (1,4); (1) Cyber-Physical Systems, DFKI GmbH, 28359 Bremen, Germany, (2) COSEDA Technologies GmbH, 01099 Dresden, Germany, (3) Institute of Computer Science, Bremen University, 28359 Bremen, Germany, (4) Institute for Complex Systems, Johannes Kepler University, 4040 Linz, Austria, MBMV-Workshop, 11.03.2025, Rostock, DE.

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Symbolic Execution of Unmodified SystemC Peripherals, Karl Aaron Rudkowski <karlaaron@uni-bremen [dot] de> (1) , Sallar Ahmadi-Pour (1) , and Rolf Drechsler (1,2), (1) Institute of Computer Science, University of Bremen, Germany, (2) Cyber-Physical Systems, DFKI GmbH, Bremen, Germany, MBMV-Workshop, 11.03.2025, Rostock, DE.

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Improving Design Generation by Interface Configuration Propagation Natalie Simson, Infineon Technologies AG and Technical University of Munich, DE, <natalie [dot] simson@infineon [dot] com>, Paritosh Kumar Sinha, Infineon Technologies AG, DE, Wolfgang Ecker, Infineon Technologies AG and Technical University of Munich, DE, MBMV-Workshop, 11.03.2025, Rostock, DE.

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Platform-Aware RTL Generation: Bridging the Gap between Design and Implementation Mohamed Badawy, Infineon Technologies AG, DE <mohamed [dot] badawy@infineon [dot] com>, Nicolas Gerlin, Paritosh Kumar Sinha, Endri Kaja, Jad Al Halabi, Stephanie Ecker, Natalie Simson, Wolfgang Ecker, Infineon Technologies AG and Technical University of Munich, DE, MBMV-Workshop, 11.3.2025, Rostock, DE.

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Parameterized Construction and Constraint-Driven Validation of Formal Hardware Specifications for Efficient Code Generation, Robert Kunzelmann, Infineon Technologies AG and Technical University of Munich, DE <robertniklas [dot] kunzelmann@infineon [dot] com>, Maximilian Berger, Infineon Technologies AG, DE and  and Technical University of Munich, DE, Wolfgang Ecker, Infineon Technologies AG and Technical University of Munich, DE, MBMV-Workshop, 11.3.2025, Rostock, DE.

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Verilator and FireSim RTL Simulations on a HPC Cluster: A Comparative Case Study, Kai Hannemann, Universität Paderborn, DE <kaiha@hni [dot] uni-paderborn [dot] de>, Hüseyin Berke Bütün, Wolfgang Mueller, Christoph J. Scheytt, MBMV-Workshop, 11.3.2025, Rostock, DE.

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Execute Your Darlings: Dynamic Execution of High-Level Formal Specifications for Validation and Early Prototyping, Robert Kunzelmann, Infineon Technologies AG and Technical University of Munich, DE, Zeyad Tahoun, Infineon Technologies AG, DE and Politecnico di Torino, IT, Wolfgang Ecker, Infineon Technologies AG and Technical University of Munich, DE, RAPIDO-Workshop @ HiPEAC, 21.1.2025, Barcelona, ES.

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P. Schmid, P. Palomero Bernardo, C. Gerum and O. Bringmann, " GOURD: Tensorizing Streaming Applications to Generate Multi-Instance Compute Platforms," in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 43, no. 11, pp. 4166-4177, 6.11.2024, https://doi.org/10.1109/TCAD.2024.3445810; [2] https://ieeexplore.ieee.org/abstract/document/10745814.

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VeriCHERI: Exhaustive Formal Security Verification of CHERI at the RTL, Anna Lena Duque Antón∗, Johannes Müller∗, Philipp Schmitz, Tobias Jauch, Alex Wezel, Lucas Deutschmann, Mohammad R. Fadiheh, Dominik Stoffel, Wolfgang Kunz, RPTU Kaiserslautern-Landau, ∗Both authors contributed equally to this research, ICCAD 2024, October 27–31, 2024, New York, NY, USA

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Keerthikumara Devarajegowda, Florian Lonsing, Mohammad R. Fadiheh, Saranyu Chattopadhyay, David Lin, Srinivas Shashank Nuthakki, Eshan Singh, Clark Barrett, Wolfgang Ecker, Wolfgang Kunz, Yanjing Li, Dominik Stoffel and Subhasish Mitra (2024), "QED and Symbolic QED: Dramatic Improvements in Pre-Silicon Verification and Post-Silicon Validation", Foundations and Trends® in Integrated Circuits and Systems: Vol. 3: No. 2–3, pp 51-217. https://dx.doi.org/10.1561/3500000003; [3] 23.20.2024

Ecker, W., Houdeau, D. et al. (2024): Edge AI: KI nahe am Endgerät. Technologie für mehr Datenschutz, Energieeffizienz und Anwendungen in Echtzeit. Whitepaper aus der Plattform Lernende Systeme, München. DOI: https://doi.org/10.48669/pls_2024-4

SIZALIZER: Multilevel Analysis Framework for Object Size Optimization, Andreas Hager-Clukas, Jonathan Schröter, and Stefan Wallentowitz, Hochschule München University of Applied Sciences, International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation (SAMOS), June 29 - July 4, 2024.

MCU-Wide Timing Side Channels and Their Detection, Johannes Müller1, Anna Lena Duque Antón1, Lucas Deutschmann1, Dino Mehmedagić1, Cristiano Rodrigues2, Daniel Oliveira2, Keerthikumara Devarajegowda3, Mohammad Rahmani Fadiheh4, Sandro Pinto2, Dominik Stoffel1, and Wolfgang Kunz1 1RPTU Kaiserslautern-Landau, 2Universidade do Minho, 3Siemens EDA, 4Stanford University, DAC 2024

Unique Program Execution Checking: Formal Security Guarantees for RISC-V Systems, Alex Wezel, Lucas Deutschmann, Tobias Jauch, Dino Mehmedagić, Johannes Müller, Mohamed Ali, Anna Lena Duque Antón, Philipp Schmitz, Mohammad Rahmani Fadiheh, Dominik Stoffel, Wolfgang Kunz, Übersichtsvortrag, RISC-V Summit Europe 2024, 24.-28.6.2024, München

Cross-Level Verification of Hardware Peripherals, Sallar Ahmadi-Pour1, Muhammad Hassan1,2, Rolf Drechsler1,2 *, 1Institute of Computer Science, University of Bremen, Germany, 2Cyber-Physical Systems, DFKI GmbH, Germany, RISC-V Summit Europe 2024, Munich, Germany 24-28 June 2024.

Luchterhandt L, Nellius T, Beck R, et al. Implementation of Different Communication Structures for a Rocket Chip Based RISC-V Grid of Processing Cells. In: MBMV 2024 - 27. Workshop Methoden Und Beschreibungssprachen Zur Modellierung Und Verifikation von Schaltungen Und Systemen“. VDE Verlag; 2024.

A Universal Specification Methodology for Quality Ensured, Highly Automated Generation of Design Models; Robert Kunzelmann1, 2, Emil Baerens1, Daniel Gerl1, 2, Mayuri Bhadra1, 2, Niklas Schwarz1, and Wolfgang Ecker1, 2; 1Infineon Technologies AG, Neubiberg, Germany; 2Technical University of Munich, Munich, Germany, MBMV 2024, 14.+15.2.2024, Kaiserslautern, Germany

Extending Clang/LLVM with Custom Instructions using TableGen – An Experience Report; Jan Schlamelcher, Thomas Goodfellow, Bewoayia Kebianyor, and Kim Grüttner, German Aerospace Center - Institute of Systems Engineering for Future Mobility, MBMV 2024, 14.+15.2.2024, Kaiserslautern, Germany

A Concise, Architecture-Focused ASIP Modeling Approach for Instruction Set Simulators; Karsten Emrich, Daniel Mueller-Gritschneder, Ulf Schlichtmann, Chair of Electronic Design Automation, Technical University of Munich, MBMV 2024, 14.+15.2.2024, Kaiserslautern, Germany

muRISCV-NN: Challenging Zve32x Autovectorization with TinyML Inference Library for RISC-V Vector Extension, Philipp van Kempen1, Jefferson Parker Jones1, Daniel Mueller-Gritschneder2, Ulf Schlichtmann1, 1Technical University of Munich, 2Vienna University of Technology, CF24-OSHW, Workshop on Open-Source Hardware, Co-located with 21th ACM International Conference on Computing Frontiers (CF’ 24) May 7 - May 9, 2024 - Ischia (NA), Italy

Longnail: High-Level Synthesis of Portable Custom Instruction Set Extensions for RISC-V Processors from Descriptions in the Open-Source CoreDSL Language, Julian Oppermann1, Brindusa Mihaela Damian-Kosterhon1, Florian Meisel1, Tammo Mürmann1, Eyck Jentzsch2, Andreas Koch1, 1Technical University of Darmstadt, 2MINRES Technologies Munich, International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), https://www.asplos-conference.org/asplos2024/ [4], San Diego, USA — April 27- May 1, 2024

Data-Oblivious and Performant: On Designing Security-Conscious Hardware, Lucas Deutschmann∗, Yazan Kazhalawi∗, Jonathan Seckinger∗, Anna Lena Duque Antón∗, Johannes Müller∗, Mohammad Rahmani Fadiheh†, Dominik Stoffel∗, Wolfgang Kunz∗; ∗RPTU Kaiserslautern-Landau, Kaiserslautern, Germany †Stanford University, Stanford, US, LATS 2024; Maceió, BR, https://cas.polito.it/LATS2024/program

TUDD Demo: ZuSE Scale4Edge – AI Hardware Accelerator for Ultra-Low-Power Keyword Spotting, ADTC + edaWorkshop24, Dresden, 9.+11.4.2024

Ein KI-Hardware-Beschleuniger für ultra-energieeffiziente Schlüsselworterkennung wird demonstriert. Durch Optimierung der Vorverarbeitung, Ausnutzung von Sparsity in einem Beschleuniger für rekurrente neuronale Netzwerke sowie einen hierarchischen Aufwachmechanismus erreichen wir eine sehr niedrige Leistungsaufnahme bei gleichzeitig hoher Klassifikationsgüte.

IHP Demo: ZuSE Scale4Edge – Der TETRISC SoC - unser RISC-V-basiertes, fehlertolerantes Mehrkernsystem auf FPGA und gefertigt als ASIC, ADTC + edaWorkshop24, Dresden, 9.+11.4.2024

Unser Demonstrator präsentiert zwei Ausführungen des adaptiven und fehlertoleranten TETRISC SoC. Zum einen umfasst er eine prototypische Implementierung auf FPGA, mit der wir gezielt Fehler einspeisen können, um die Fehlertoleranz des Systems zu demonstrieren. Zum anderen präsentieren wir die finale Version, gefertigt in IHP 130nm Technologie. Diese zeigt die Realisierbarkeit und Funktionalität des Systems und ermöglicht Messungen zur Geschwindigkeit und Stromaufnahme.

UFR Demo: ZuSE Scale4Edge – Software-based Self-Test Generation for RISC-V, FPGA-basierter Demonstrator

Ein FPGA-basierter Demonstrator mit einem RISC-V Prozessorkern, welcher die LED-Anzeigen auf der Demoplatine steuert und periodisch einen Selbsttest ausführt. Die SBST ist für den Test der Arithmetic Logic Unit (ALU) und die Registerbank des verwendeten RISC-V Prozessorkernes ausgelegt. Über Schalter können ausgewählte Fehler in den Prozessorkern injiziert werden, welcher dann mittels des SBSTs diese detektiert, und auf den Anzeigen das Testergebnis signalisiert.

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Poster: Trust & Security-Forschungen in Scale4Edge und VE-VIDES durch die Werkzeuge Questa Verify Secure und Questa Verify Trust, Jörg Bormann, Siemens EDA, ADTC + edaWorkshop24, Dresden, 9.+11.4.2024

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TUDD-Poster: AI Hardware Accelerator for Ultra-Low-Power Keyword Spotting, Johannes Partzsch, TU Dresden, ADTC + edaWorkshop24, Dresden, 9.+11.4.2024

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TUDD-Demo: AI Hardware Accelerator for Ultra-Low-Power Keyword Spotting, Johannes Partzsch, TU Dresden, ADTC + edaWorkshop24, Dresden, 9.+11.4.2024

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A Golden-Free Formal Method for Trojan Detection in Non-Interfering Accelerators, Anna Lena Duque Antón1, Johannes Müller1, Lucas Deutschmann1, Mohammad Rahmani Fadihehy2, Dominik Stoffel1, Wolfgang Kunz1; 1University of Kaiserslautern-Landau, Kaiserslautern, Germany 2Stanford University, Stanford, USA, DATE 2024

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A Scalable RISC-V Hardware Platform for Intelligent Sensor Processing; Paul Palomero Bernardo, Patrick Schmid, Oliver Bringmann, University of Tübingen, Mohammed Iftekhar, Babak Sadiye, Wolfgang Müller Paderborn University / Heinz Nixdorf Institute, Andreas Koch, Technical University of Darmstadt, Eyck Jentzsch, MINRES Technologies GmbH, Axel Sauer, Ingo Feldner, Robert Bosch GmbH, Wolfgang Ecker, Infineon Technologies AG; 25.-27.3.2024 at Design, Automation and Test in Europe (DATE) Conference 2024, Valencia, ES (https://date24.date-conference.com/programme [5]).

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A Scalable Formal Verification Methodology for Data-Oblivious Hardware, Lucas Deutschmann1, Johannes Müller1, Mohammad R. Fadiheh2, Dominik Stoffel1, and Wolfgang Kunz1; 1University of Kaiserslautern-Landau, Kaiserslautern, Germany 2Stanford University, Stanford, USA, TCAD 2024; https://doi.org/10.1109/TCAD.2024.3374249

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J. Kappes, R. Kunzelmann, K. Emrich, C. Foik, D. Mueller-Gritschneder and W. Ecker, Effective Processor Model Generation from Instruction Set Simulator to Hardware Design, 2023 IEEE Nordic Circuits and Systems Conference (NorCAS), Aalborg, Denmark, 2023, pp. 1-7, https://doi.org/10.1109/NorCAS58970.2023.10305465.

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A RISC-V MCU with adaptive reverse body bias and ultra-low-power retention mode in 22 nm FD-SOI; Heiner Bauer, Marco Stolba, Stefan Scholze, Dennis Walter, Christian Mayr, Electrical and Computer Engineering Dept., TU Dresden, Germany, Alexander Oefelein, Sebastian Höppner, André Scharfe, Flo Schraut, Holger Eisenreich, Racyics GmbH, Dresden, Germany, 20th International SoC Conference (ISOCC 2023) will be held from October 25 to 28, 2023 at at the Ramada Plaza Jeju Hotel in Jeju Island, Korea, https://isocc.org.

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N. I. Deligiannis, T. Faller, I. Guglielminetti, R. Cantoro, B. Becker, M. S. Reorda, Automatic Identification of Functionally Untestable Cell-Aware Faults in Microprocessors, to be published on 2023 IEEE 32nd Asian Test Symposium (ATS), October 14-17, 2023, Beijing, China

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Minimally Invasive Generation of RISC-V Instruction Set Simulators from Formal ISA Models; Sören Tempel1 Tobias Brandt Christoph Lüth1,2 Rolf Drechsler1,2; 1Institute of Computer Science, University of Bremen, Germany; 2Cyber-Physical Systems, DFKI GmbH, Bremen, Germany; FDL 2023

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Virtual Prototype driven Application Specific Hardware Optimization; Jan Zielasko1 Rolf Drechsler1,2; 1Cyber-Physical Systems, DFKI GmbH, Germany; 2Institute of Computer Science, University of Bremen, Germany; FDL 2023

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Identification of ISA-Level Mutation-Classes for Qualification of RISC-V Formal Verification, Milan Funck1 Sallar Ahmadi-Pour2 Vladimir Herdt1,2 Rolf Drechsler1,2; 1Cyber-Physical Systems, DFKI GmbH, Bremen, Germany; 2Institute of Computer Science, University of Bremen, Bremen, Germany; FDL 2023

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A RISC-V based platform supporting mixed timing-critical and high performance workloads, Mehrdad Poorhosseini, University of Oldenburg, Kim Grüttner, German Aerospace Center (DLR), 26th Euromicro Conference on Digital System Design (DSD) in Durres, Albania, Sept. 6th – Sept. 8th, 2023.

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Efficient ML-Based Performance Estimation Approach across Different Microarchitectures for RISC-V Processors, Weiyan Zhang1 Mehran Goli2 Muhammad Hassan1,2 Rolf Drechsler1,2, 1Cyber-Physical Systems, DFKI GmbH, 2Institute of Computer Science, University of Bremen, 26th Euromicro Conference on Digital System Design (DSD) in Durres, Albania, Sept. 6th – Sept. 8th, 2023.

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The TETRISC SoC - A resilient Quad-Core System based on the ResiliCell approach, Markus Ulbricht a, Li Lu a, Junchao Chen a, Milos Krstic a b, a

IHP - Leibniz Institute for High Performance Microelectronics, b University of Potsdam, Received 2 June 2023, Revised 24 July 2023, Accepted 28 July 2023, Available online 14 August 2023, Version of Record 14 August 2023., Microelectronics Journal, https://doi.org/10.1016/j.microrel.2023.115173.

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Design of Access Control Mechanisms in Systems-on-Chip with Formal Integrity Guarantees; Dino Mehmedagić, Mohammad Rahmani Fadiheh, Johannes Müller, Anna Lena Duque Antón, Dominik Stoffel, Wolfgang Kunz, Department of Electrical and Computer Engineering, Rheinland-Pfälzische Technische Universität (RPTU) Kaiserslautern-Landau, Germany, 32nd USENIX Security Symposium, 9.-11.8.2023, in Anaheim, CA, USA

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RISC-V Timing-Instructions for Open Time-Triggered Architectures, Nithin Ravani Nanjundaswamy, Gregor Nitsche, Frank Poppen (now: NXP Semiconductors Germany GmbH, Hamburg), Kim Grüttner, German Aerospace Center, Oldenburg, Germany, VERDI 2023, 1st International Workshop on Verification & Validation of Dependable Cyber-Physical Systems, 27 June 2023, Porto, Portugal, Co-located with DSN 2023

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Liyuan Guo, Matthias Jobst, Johannes Partzsch, Stefan Scholze, Andreas Dixius, Matthias Lohrmann, Seyed Mohammad Ali Zeinolabedin, Christian Mayr: A Low-Power Hardware Accelerator of MFCC Extraction for Keyword Spotting in 22nm FDSOI, Konferenz „Artificial Intelligence Circuits and Systems“ (AICAS) 2023

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The TETRISC SoC - A resilient quad-core system based on Pulpissimo, Markus Ulbricht1, Junchao Chen1, Li Lu1 and Milos Krstic1,2, 1IHP - Leibniz Institute for High Performance Microelectronics, Frankfurt (Oder), Germany, 2University of Potsdam, Potsdam, Germany, RISC-V Summit Europe 2023, Barcelona, Spain, 5.-9.6.2023

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Automated Cross-level Verification Flow of a Highly Configurable RISC-V Core Family with Custom Instructions, Stanislaw Kaushanski, Eyck Jentzsch, MINRES Technologies GmbH, Germany, RISC-V Summit Europe 2023, Barcelona, Spain, 5.-9.6.2023

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Scale4Edge – Scaling RISC-V for Edge Applications, Wolfgang Ecker1, Milos Krstic2,3, Markus Ulbricht2, Andreas Mauderer4, Eyck Jentzsch5, Andreas Koch6, Bastian Koppelmann7, Wolfgang Mueller7, Babak Sadiye7, Niklas Bruns8, Rolf Drechsler8, Daniel Mueller-Gritschneder9, Jan Schlamelcher10, Kim Grüttner10, Jörg Bormann11, Wolfgang Kunz12, Reinhold Heckmann13, Gerhard Angst14, Ralf Wimmer14, Bernd Becker15, Tobias Faller15, Paul Palomero Bernardo16, Oliver Bringmann16, Johannes Partzsch17, Christian Mayr17, 1Infineon Technologies AG, 2IHP – Leibniz Institut für innovative Mikroelektronik, 3University Potsdam, 4Robert Bosch GmbH, 5MINRES Technologies GmbH, 6Technical University of Darmstadt, 7Heinz Nixdorf Institute/Paderborn University, 8University of Bremen / DFKI GmbH, 9Technical University of Munich, 10German Aerospace Center (DLR), 11Siemens EDA, 12Technische Universität Kaiserslautern, 13AbsInt Angewandte Informatik GmbH, 14Concept Engineering GmbH, 15Albert-Ludwigs-Universität Freiburg, 16Universität Tübingen, 17Technische Universität Dresden, RISC-V Summit Europe 2023, Barcelona, Spain, 5.-9.6.2023

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Extended Abstract: Automated Generation of a RISC-V LLVM Toolchain for Custom MACs, Philipp van Kempen1∗, Karsten Emrich1, Daniel Mueller-Gritschneder1 and Ulf Schlichtmann1, 1School of Computation, Information and Technology, Technical University of Munich, RISC-V Summit Europe 2023, Barcelona, Spain, 5.-9.6.2023

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Extended Abstract: A Flexible Simulation Environment for RISC-V, Karsten Emrich1, Conrad Foik1, Johannes Kappes2, Sebastian Prebeck2, Daniel Mueller-Gritschneder1, Wolfgang Ecker2, Ulf Schlichtmann1, 1Technical University of Munich, Germany 2Infineon Technologies, RISC-V Summit Europe 2023, Barcelona, Spain, 5.-9.6.2023

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T. Faller, N. Deligiannis, M. Schwörer, M. S. Reorda, B. Becker, Constraint-Based Automatic SBST Generation for RISC-V Processor Families, 28th IEEE European Test Symposium 2023, 22-26 May 2023, Venezia, Italy

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J. Anders, P. Andreu, B. Becker, S. Becker, R. Cantoro, N. I. Deligiannis, N. Elhamawy, T. Faller, C. Hernandez, N. Mentens, M. N. Rizi, I. Polian, A. Sajadi, M. Sauer, D. Schwachhofer, M. S. Reorda, T. Stefanov, I. Tuzov, S. Wagner, N. Zidari, A Survey of Recent Developments in Testability, Safety and Security of RISC-V Processors, 28th IEEE European Test Symposium 2023, 22-26 May 2023, Venezia, Italy

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PULP Fiction No More - Dependable PULP Systems for Space; Markus Ulbricht∗, Yvan Tortorella†, Michael Rogenmoser‡, Li Lu∗, Junchao Chen∗, Francesco Conti†, Milos Krstic∗§, Luca Benini†‡; ∗IHP - Leibniz Institute for High Performance Microelectronics, DE, †DEI Department, University of Bologna, IT, ‡Integrated Systems Laboratory (IIS), ETH Zürich, CH, §University of Potsdam, Potsdam, DE at 28th IEEE European Test Symposium (ETS) 2023 on May 22-26 in Venice, IT

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A Survey of Recent Developments in Testability, Safety and Security of RISC-V Processors; Jens Anders, Pablo Andreu, Bernd Becker, Steffen Becker, Riccardo Cantoro, Nikolaos I.Deligiannis, Nourhan Elhamawy, Tobias Faller, Carles Hernandez, Nele Mentens, Mahnaz Namazi Rizi, Ilia Polian, Abolfazl Sajadi, Mathias Sauer, Denis Schwachhofer, Matteo Sonza Reorda, Todor Stefanov, Ilya Tuzov, Stefan Wagner and Nuša Zidarič; 2023 IEEE European Test Symposium (ETS), Venezia, Italy, 2023, pp. 1-10, https://doi.org/10.1109/ETS56758.2023.10174099.

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Constraint-Based Automatic SBST Generation for RISC-V Processor Families; Tobias Faller∗, Nikolaos I. Deligiannis†, Markus Schwörer∗, Matteo Sonza Reorda†, Bernd Becker∗, ∗University of Freiburg, Department of Computer Science - Freiburg, Germany, †Politecnico di Torino, Department of Control and Computer Engineering (DAUIN) - Turin, Italy, ETS 2023

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Efficient Software-Implemented HW Fault Tolerance for TinyML Inference in Safety-critical Applications; Uzair Sharif, Daniel Mueller-Gritschneder,

Rafael Stahl, Ulf Schlichtmann, Chair of Electronic Design Automation, Technical University of Munich (TUM), Munich, Germany at Design, Automation and Test in Europe (DATE) Conference 2023, Antwerp, BE

Best Paper Award Candidate: Processor Verification using Symbolic Execution: A RISC-V Case-Study; Niklas Bruns, Vladimir Herdt and Rolf Drechsler; Universität Bremen, Design, Automation and Test in Europe (DATE) Conference 2023, Antwerp, BE

Fused Depthwise Tiling for Memory Optimization in TinyML Deep Neural Network Inference; Rafael Stahl, Daniel Mueller-Gritschneder, Ulf Schlichtmann, Technical University of Munich, Germany, TinyML Research Symposium 2023

Luchterhandt, Lars; Nellius, Tom; Beck, Robert; Dömer, Rainer; Kneuper, Pascal; Mueller, Wolfgang; Sadiye, Babak. Towards a Rocket Chip Based Implementation of the RISC-V GPC Architecture. In: Workshop Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen (MBMV 2023), IEEE Xplore, 18. - 19. Mrz. 2023.

N. I. Deligiannis, T. Faller, R. Cantoro, T. Paxian, B. Becker and M. S. Reorda, Automating the Generation of Programs Maximizing the Repeatable Constant Switching Activity in Microprocessor Units via MaxSAT, in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, https://doi.org/10.1109/TCAD.2023.3252467.

Specification-based Symbolic Execution for Stateful Network Protocol Implementations in the IoT. Sören Tempel, Vladimir Herdt, Rolf Drechsler, IEEE Internet of Things Journal 2023; https://doi.org/10.1109/JIOT.2023.3236694

Versatile and Flexible Modelling of the RISC-V Instruction Set Architecture; Sören Tempel1, Tobias Brandt3, and Christoph Lüth1,2; 1University of Bremen, DE; 2Deutsches Forschungszentrum für Künstliche Intelligenz (DFKI), DE; 3tobbra91@gmail [dot] com; TFP (and TFPIE) 2023, 24th International Symposium on Trends in Functional Programming, 12 - 15 January 2023, UMass Boston, Boston, MA, USA; https://trendsfp.github.io/schedule.html

IEEE Top Pick in Security: Fadiheh, M. R., Wezel, A., Müller, J., Bormann, J., Ray, S., Fung, J. M., Mitra, S., Stoffel, D., & Kunz, W. (2023, January). An Exhaustive Approach to Detecting Transient Execution Side Channels in RTL Designs of Processors, in IEEE Transactions on Computers, vol. 72, no. 1, pp. 222-235, 1 Jan. 2023, doi: 10.1109/TC.2022.3152666

Koch, A. SCAIE-V: A Scalable Open-Source Interface for Flexible and Portable ISA Extensions. Invited talk at RISC-V Summit 2022; https://riscvsummit2022.sched.com/event/1CD6J/scaie-v-a-scalable-open-source-interface-for-flexible-and-portable-isa-extensions-andreas-koch-tu-darmstadt

N. I. Deligiannis, T. Faller, J. E. Rodriguez Condia, R. Cantoro, B. Becker and M. S. Reorda, Using Formal Methods to Support the Development of STLs for GPUs, 2022 IEEE 31st Asian Test Symposium (ATS), Taichung City, Taiwan, 2022, pp. 84-89, https://doi.org/10.1109/ATS56056.2022.00027.

The TetRISC SoC for reliability critical applications, J. Chen, U. Markus, Presentation, the 5th Workshop on RISC-V Activities, Berlin, Germany, 7.11.2022

Präsentation: OPTI-RISK: Design of an Optical Probing Attack Hardened RISC-V Core with an Industrially Compatible CMOS Gate Library. Sajjad Parvin, Sallar Ahmadi-Pour, Chandan Kumar Jha, Frank Sill Torres, and Rolf Drechsler. 5th RISC-V Activity Workshop 2022

Schlamelcher, Jan und Grüttner, Kim (2022) A DSL based approach for supporting custom RISC-V instruction extensions in LLVM. 5th Workshop on RISC-V Activities, Berlin, Deutschland.

Ravani Nanjundaswamy, Nithin und Grüttner, Kim (2022) Timing-Anweisungen für RISC-V-basierte Hard Real Time Edge Devices 5th Workshop on RISC-V Activities, Berlin, Deutschland.

Wolfgang Kunz: „Spectres, Meltdowns, Zombies, Orcs: Can formal methods banish the ghosts that haunt your hardware?" Keynote; 5th Workshop on RISC-V Activities, Berlin, Germany, 7.11.2022

Applying GNNs to Timing Estimation at RTL. Daniela Sanchez Lopera, Wolfgang Ecker: ICCAD 2022: 3

SISL: Concolic Testing of Structured Binary Input Formats via Partial Specification, Sören Tempel1, Vladimir Herdt1,2, and Rolf Drechsler1,2, 1 Institute of Computer Science, University of Bremen, 28359 Bremen, Germany, 2 Cyber-Physical Systems, DFKI GmbH, 28359 Bremen, Germany, ATVA 2022, Oct 25, 2022 - Oct 28, 2022, Beijing, China

MetaFS: Model-driven Fault Simulation Framework. Endri Kaja, Nicolas Gerlin, Monideep Bora, Keerthikumara Devarajegowda, Dominik Stoffel, Wolfgang Kunz, Wolfgang Ecker. 2022 IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT); 19-21 October 2022

The MicroRV32 framework: An Accessible and Configurable Open Source RISC-V Cross-Level Platform for Education and Research. Sallar Ahmadi-Pour, Vladimir Herdt, Rolf Drechsler. Journal of Systems Architecture (JSA) 2022, Journal. https://doi.org/10.1016/j.sysarc.2022.102757

A framework that enables systematic analysis of mixed-signal applications on FPGA. Gabriel Rutsch, Maximilian Groebner, Anthony Sanders, Konrad Maier, Wolfgang Ecker; 2022 IEEE International Workshop on Rapid System Prototyping (RSP); RSP 2022: 50-56; https://doi.org/10.1109/RSP57251.2022.10039031

Philipp van Kempen, Rafael Stahl, Daniel Müller-Gritschneder and Ulf Schlichtmann MLonMCU: TinyML Benchmarking with Fast Retargeting, In: CODAI 2022 Workshop on Compilers, Deployment, and Tooling for Edge AI, 13.10.2022; https://doi.org/10.1145/3615338.3618128

Design of a Tightly-Coupled RISC-V Physical Memory Protection Unit for Online Error Detection. Nicolas Gerlin, Endri Kaja, Monideep Bora, Keerthikumara Devarajegowda, Dominik Stoffel, Wolfgang Kunz, Wolfgang Ecker: VLSI-SoC 2022: 1-6

Fast and Accurate Model-Driven FPGA-based System-Level Fault Emulation. Endri Kaja, Nicolas Gerlin, Monideep Bora, Gabriel Rutsch, Keerthikumara Devarajegowda, Dominik Stoffel, Wolfgang Kunz, Wolfgang Ecker: VLSI-SoC 2022: 1-6

Advanced Embedded System Modeling and Simulation in an Open Source RISC-V Virtual Prototype. Pascal Pieper, Vladimir Herdt and Rolf Drechsler. Journal of Low Power Electronics and Applications (JLPEA) 2022. https://doi.org/10.3390/jlpea12040052

Transformative Hardware Design following the Model-Driven Architecture Vision, Zhao Han1,2, Gabriel Rutsch1, Deyan Wang1,2, Bowen Li1,2, Sebastian Siegfried Prebeck1,2, Daniela Sanchez Lopera1,2,Keerthikumara Devarajegowda1, and Wolfgang Ecker1,2; 1 Infineon Technologies AG, Germany; 2 Technical University Munich, Germany; Part of Springer Book; https://doi.org/10.1007/978-3-031-16818-5_3

Präsentation: Symbolic Execution for RISC-V Embedded Software Using SystemC Peripheral Models. Autor: Sören Tempel, Vladimir Herdt, Rolf Drechsler, 3rd International KLEE Workshop on Symbolic Execution 2022, Great Britain

Unified HW/SW Coverage: A Novel Metric to Boost Coverage-guided Fuzzing for Virtual Prototype based HW/SW Co-Verification, 1st Niklas Bruns, Institute of Computer Science University of Bremen, Bremen, Germany, 2nd Vladimir Herdt, Institute of Computer Science University of Bremen, Cyber-Physical Systems, DFKI GmbH, Bremen, Germany, 3rd Rolf Drechsler, Institute of Computer Science, University of Bremen, Cyber-Physical Systems, DFKI GmbH, Bremen, Germany, FDL 2022, September 14–16, 2022, Linz, Austria

3D Visualization of Symbolic Execution Traces, Jan Zielasko1 S¨oren Tempel2 Vladimir Herdt1,2 Rolf Drechsler1,2, 1Cyber-Physical Systems, DFKI GmbH, 28359 Bremen, Germany, 2Institute of Computer Science, University of Bremen, 28359 Bremen, Germany, FDL 2022, September 14–16, 2022, Linz, Austria

CorePerfDSL: A Flexible Processor Description Language for Software Performance Simulation Conrad Foik, Daniel Mueller-Gritschneder, Ulf Schlichtmann, Technical University of Munich, Germany, FDL 2022, September 14–16, 2022, Linz, Austria

Industrial Experience with Open-Source EDA Tools. Christian Lück, Daniela Sanchez Lopera, Sven Wenzek, Wolfgang Ecker: MLCAD 2022: 143

Präsentation: Automated Testing of RIOT modules using SymEx-VP. Sören Tempel, Vladimir Herdt, Rolf Drechsler. RIOT Summit 2022, Germany

Wolfgang Ecker organisierte die Session “Industrial Sesson: RISC-V: Evolution, Innovation and Research Challenges of Open-ISA” zur IEEE 35th International System-on-Chip Conference (SOCC) ; Titanic, Belfast, Northern Ireland, September 5-8, 2022; https://edas.info/p29519#S1569607348; [6] https://www.ieee-socc.org/

An Industrial Perspective on RISC-V Innovation by Keerthikumara Devarajegowda, Sebastian Prebeck, Endri Kaja, Nicolas Gerlin, Sven Wenzeck, Daniela Sanchez Lopera, Wolfgang Ecker from Infineon Technologies; IEEE 35th International System-on-Chip Conference (SOCC); Titanic, Belfast, Northern Ireland, September 5-8, 2022

Intel Hardware Security Academic Award 2022; Winner First place: “A Formal Approach to Confidentiality Verification in SoCs at the Register Transfer Level”; Johannes Müller1, Mohammad R. Fadiheh1, Anna Lena Duque Antón1, Thomas Eisenbarth2, Dominik Stoffel1, Wolfgang Kunz1, 1Technische Universität Kaiserslautern, DE, 2Universität zu Lübeck, DE (https://www.intel.com/content/www/us/en/security/security-practices/secu... [7]); https://doi.org/10.1109/DAC18074.2021.9586248; [8] 16.8.2022

Verifying SystemC TLM Peripherals using Modern C++ Symbolic Execution Tools; Pascal Pieper1, Vladimir Herdt12, Daniel Große3, Rolf Drechsler12; 1Cyber-Physical Systems, DFKI GmbH, Bremen, Germany; 2 Institute of Computer Science, University of Bremen, Bremen, Germany; Institute for Complex Systems, Linz, Austria; DAC 2022, 10.-14.7.2022

HIPEAC-Award: SCAIE-V: An Open-Source SCAlable Interface for ISA Extensions for RISC-V Processors; Mihaela Damian1, Julian Oppermann1,

Christoph Spang1, Andreas Koch1; 1Technical University Darmstadt, Darmstadt, Germany; DAC 2022, 10.-14.7.2022, https://doi.org/10.1145/3489517.3530432

DAC-2022 Best Paper Award: Towards a Formally Verified Hardware Root-of-Trust for Data-Oblivious Computing, Lucas Deutschmann, Johannes Müller, Mohammad R. Fadiheh, Dominik Stoffel, Wolfgang Kunz, TU Kaiserslautern, DAC 2022, 10.-14.7.2022

L. Lu, J. Chen, M. Ulbricht and M. Krstic, A Methodology for Identifying Critical Sequential Circuits with Graph Convolutional Networks, 2022 IEEE Computer Society Annual Symposium on VLSI (ISVLSI), 2022, pp. 20-25, https://doi.org/10.1109/ISVLSI54635.2022.00017.

A Smart HW-Accelerator for Non-uniform Linear Interpolation of ML-Activation Functions. Sebastian Siegfried Prebeck, Wafic Lawand, Mounika Vaddeboina, Wolfgang Ecker: SAMOS 2022: 267-282

Dariol, Quentin und Le Nours, Sebastien und Pillement, Sebastien und Stemmer, Ralf und Helms, Domenik und Grüttner, Kim (2022) A Hybrid Performance Prediction Approach for Fully-Connected Artificial Neural Networks on Multi-core Platforms. In: 22nd International Conference on Embedded Computer Systems: Architectures, Modeling, and Simulation, SAMOS 2022, 13511, Seiten 250-263. Eingebettete Computersysteme: Architectures, Modeling, and Simulation - SAMOS 2022, 3-7 Juli 2022, Samos, Griechenland. https://doi.org/10.1007/978-3-031-15074-6_16 [9], ISBN 978-303115073-9, ISSN 0302-9743.

Reliability Evaluation of General Purpose and AI Processing Architectures, M. Krstic, Invited Presentation, 10th Prague Embedded Systems Workshop (PESW 2022), Horomerice, June 30 - July 02, 2022, Czech Republic

Poster: Philipp van Kempen, Rafael Stahl, Daniel Mueller-Gritschneder TinyML: Bringing Deep Learning to Ultra-low-power Microcontrollers, TUM Industry Day 2022

tinyML Class auf der Embedded World Konferenz 2022, TUM, embedded World, Nuremberg, Germany, 21.6.2022

Bringing TinyML to RISC-V With Specialized Kernels and a Static Code Generator Approach, Rafael Stahl (Technical University of Munich), embedded World, Nuremberg, Germany, 21.6.2022

Advanced Environment Modeling and Interaction in an Open Source RISC-V Virtual Prototype; Pascal Pieper1, Vladimir Herdt12, Rolf Drechsler12, 1Cyber-Physical Systems, DFKI GmbH, 2Institute of Computer Science, University of Bremen; GLSVLSI 2022; June 6-8, 2022, Irvine, CA, US

Efficient Cross-Level Processor Verification using Coverage-guided Fuzzing; Niklas Bruns1, Vladimir Herdt12, Daniel Große23, Rolf Drechsler12, 1Institute of Computer Science, University of Bremen 2Cyber-Physical Systems, DFKI GmbH, 3Johannes Kepler University; GLSVLSI 2022; June 6-8, 2022, Irvine, CA, US

Reliability in AI Processing, M. Krstic, Invited Presentation, Workshop "Com-In-AI", Faculty of Electronic Engineering, Nis, May 31, 2022, Serbia

Design of FPGA-based System with Supervised Machine Learning for Solar Particle Event Prediction, R. Saric, J. Chen, E. Custovic, G. Panic, J. Kevric, D. Jokic, M. Krstic, Presentation, 17th IFAC Conference on Programmable Devices and Embedded Systems (PDeS 2022), Sarajevo, May 17 - 19, 2022, Bosnia and Herzegovina, https://doi.org/10.1016/j.ifacol.2022.06.038.

Fast Error Propagation Probability Estimates by Answer Set Programming and Approximate Model Counting; ANSELM BREITENREITER1, MARKO ANDJELKOVIC1, OLIVER SCHRAPE1 AND MILOS KRSTIC1,2; 1IHP – Leibniz-Institut für innovative Mikroelektronik, Frankfurt (Oder), Germany, 2University of Potsdam, Potsdam, Germany; Corresponding author: Anselm Breitenreiter in IEEE Access, vol. 10, pp. 51814-51825, 2022, https://doi.org/10.1109/ACCESS.2022.3174564.

Oppermann, J., Urbach, M., Demme, J. How to Make Hardware with Maths: An Introduction to CIRCT's Scheduling Infrastructure. Presentation at European LLVM Developer’s Meeting (EuroLLVM) 2022; https://www.youtube.com/watch?v=tctEk7O5DU0

Towards Quantification and Visualization of the Effects of Concretization during Concolic Testing; Sören Tempel1, Vladimir Herdt1,2, Rolf Drechsler1,2, 1Institute of Computer Science, University of Bremen; 2Cyber-Physical Systems, DFKI GmbH, Bremen; IEEE Embedded Systems Letters (ESL) journal; 2022; https://doi.org/10.1109/LES.2022.3171603

Identifying Critical Flip-flops in Circuits with Graph Convolutional Networks, L. Lu, J. Chen, M. Ulbricht, M. Krstic, Presentation and Published Paper, IEEE International Symposium on Design and Diagnostics of Electronic Circuits and Systems (DDECS 2022), Prague, April 06 - 08, 2022, Czech Republic; https://ddecs2022.fit.cvut.cz/main/?sec=prog#page_header

Sensing and Predicting Solar Particle Events, J.-C. Chen, Presentation, Workshop of BB-KI-Chips Project, online, March 31, 2022, Germany

SymEx-VP: An Open Source Virtual Prototype for OS-Agnostic Concolic Testing of IoT Firmware; Sören Tempel1 Vladimir Herdt1,2 Rolf

Drechsler1,2; 1Institute of Computer Science, University of Bremen, Bremen, Germany; 2Cyber-Physical Systems, DFKI GmbH, Bremen, Germany; Journal of Systems Architecture (JSA); Vol. 125; April 2022; https://doi.org/10.1016/j.sysarc.2022.102456.

---

The Scale4Edge RISC-V Ecosystem, Wolfgang Ecker, Infineon Technologies AG; Milos Krstic, IHP –Leibniz Institut für innovative Mikroelektronik & University Potsdam; Andreas Mauderer, Robert Bosch GmbH; Eyck Jentzsch, MINRES Technologies GmbH; Mihaela Damian, Julian Oppermann, Andreas Koch, Technical University of Darmstadt; Peer Adelt, Wolfgang Müller, Paderborn University; Vladimir Herdt, Rolf Drechsler, University of Bremen / DFKI GmbH; Rafael Stahl, Karsten Emrich, Daniel Müller-Gritschneder, Technical University of Munich; Jan Schlamelcher, Kim Grüttner, OFFIS - Institut für Informatik; Jörg Bormann, Siemens EDA; Wolfgang Kunz, Technische Universität Kaiserslautern; Reinhold Heckmann, AbsInt Angewandte Informatik GmbH; Gerhard Angst, Ralf Wimmer, Concept Engineering GmbH; Bernd Becker, Philipp Scholl, Albert-Ludwigs-Universität Freiburg; Paul Palomero Bernardo, Oliver Bringmann, Universität Tübingen; DATE 2022, 14.3-23.3.2022; Online. https://doi.org/https://doi.org/10.23919/DATE54114.2022.9774593

---

Cross-Level Processor Verification via Endless Randomized Instruction Stream Generation with Coverage-guided Aging, Niklas Bruns1 Vladimir Herdt1;2 Eyck Jentzsch3 Rolf Drechsler1;2, 1Institute of Computer Science, University of Bremen, 28359 Bremen, Germany, 2Cyber-Physical Systems, DFKI GmbH, 28359 Bremen, Germany, 3MINRES Technologies GmbH, 85579 Neubiberg, Germany; DATE 2022, 14.3-23.3.2022; Online

---

ZuSE Scale4Edge: Entwicklungsplattform und Ökosystem für skalierbare Spezialprozessoren im Edge-Computing - Das etwas andere Projekt, Wolfgang Ecker, Infineon Technologies, Digitale Fachkonferenz „Vertrauenswürdige Elektronik 2022“, 9.3.2022

---

Gewinner des Nachwuchswettbewerbs zur Digitale Fachkonferenz „Vertrauenswürdige Elektronik 2022“: Rahmani Fadiheh (Technische Universität Kaiserlautern): Microarchitectural side channels and security-critical design bugs: Towards a unified approach for RTL Hardware verification, 9.+10.3.2022, Online

---

Formal Verification of Highly Parametrized SoC-Designs; A. Paule, VLSI 2022 Very-large-scale integration Seminar

---

Constraints for Automatic, Generic SBST Generation for RISC-V Using SAT-Solving; Tobias Faller, Markus Schwörer, Philipp Scholl, Tobias Paxian, and Bernd Becker; Chair of Computer Architecture University of Freiburg, TuZ 2022, Bremerhaven, 27.02. bis 01.03.2022

---

Mohammad R. Fadiheh, Alex Wezel, Johannes Müller, Jörg Bormann, Sayak Ray, Jason M. Fung, Subhasish Mitra, Dominik Stoffel, Wolfgang Kunz: An Exhaustive Approach to Detecting Transient Execution Side Channels in RTL Designs of Processors, IEEE Transactions on Computers, February 2022; https://doi.org/10.1109/TC.2022.3152666.

---

A Scalable, Configurable and Programmable Vector Dot-Product Unit for Edge AI, Sebastian Prebeck, Sathya Ashok, Mounika Vaddeboina, Keerthikumara Devarajegowda, and Wolfgang Ecker Infineon Technologies AG, Munich, Germany, MBMV 2022, Online, 17.2.2022

---

RISC-V Processor Verification with Coverage-guided Aging; Niklas Bruns1, Vladimir Herdt1;2, Eyck Jentzsch3, Rolf Drechsler1;2; 1Institute of Computer Science, University of Bremen, Germany; 2Cyber-Physical Systems, DFKI GmbH, Bremen, Germany; 3MINRES Technologies GmbH, 85579 Neubiberg, Germany; MBMV 2022, Online, 17.2.2022

---

Solar Particle Event and Single Event Upset Prediction from SRAM-based Monitor and Supervised Machine Learning, J.-C. Chen, T. Lange, M. Andjelkovic, A. Simevski, L. Lu, M. Krstic, Published Paper, IEEE Transactions on Emerging Topics in Computing

---

J. Chen, T. Lange, M. Andjelkovic, A. Simevski, L. Lu and M. Krstic, Solar Particle Event and Single Event Upset Prediction from SRAM-Based Monitor and Supervised Machine Learning, in IEEE Transactions on Emerging Topics in Computing, vol. 10, no. 2, pp. 564-580, 1 April-June 2022, https://doi.org/10.1109/TETC.2022.3147376.

---

Automated Detection of Spatial Memory Safety Violations for Constrained Devices, Sören Tempel1 Vladimir Herdt1;2 Rolf Drechsler1;2, 1Institute of Computer Science, University of Bremen, Bremen, Germany, 2Cyber-Physical Systems, DFKI GmbH, Bremen, Germany, ASP-DAC 2022, 17.-20.1.2022

---

Advanced Virtual Prototyping for Cyber-Physical Systems using RISC-V: Implementation, Verification and Challenges; Vladimir Herdt1,2* & Rolf Drechsler1,2; 1Institute of Computer Science, University of Bremen, Bremen 28359, Germany; 2Cyber-Physical Systems, DFKI GmbH, Bremen 28359, Germany, In Journal Science China Information Sciences (SCIS) - https://doi.org/10.1007/s11432-020-3308-4 [10], 23.12.2021

---

Johannes Müller, Mohammad R. Fadiheh, Anna Duque Anton, Thomas Eisenbarth, Dominik Stoffel, Wolfgang Kunz :“A Formal Approach to Confidentiality Verification in SoCs at the Register Transfer Level”, IEEE/ACM Design Automation Conference (DAC), Dec. 5-9, 2021, San Francisco/virtual, USA.

---

Towards Reliable Spatial Memory Safety for Embedded Software by Combining Checked C with Concolic Testing, Universität Bremen, DAC 2021, December 5-9, 2021, virtual

---

Panel: The RISC-V Software Ecosystem: Where we are and where are we going?, Ingo Feldner (Bosch, D), Drew Fustini (Beagleboard, US), Mark Himelstein (RISC-V International, CH), Philipp Tomisch (TU Vienna and VRULL GmbH, AT) 4th Workshop on RISC-V Activities, Online, 02.12.2021

Setting up a debug solution with Lauterbach Debug Hardware and Software for a custom implementation of a RISC-V core - Lessons Learned, Zhao Han (Infineon, D), 4th Workshop on RISC-V Activities, Online, 02.12.2021

Verification of RISC-V Embedded Software by Integrating Concolic Testing with SystemC-based Virtual Prototypes, Sören Tempel (University of Bremen, D), Vladimir Herdt (University of Bremen / DFKI, D), Rolf Drechsler (University of Bremen / DFKI, D), 4th Workshop on RISC-V Activities, Online, 02.12.2021

Extending the RISC-V LLVM backend to Support Fault-tolerant Computing, Uzair Sharif (Technical University of Munich, D), 4th Workshop on RISC-V Activities, Online, 02.12.2021

The TETRISC SoC for safety critical applications, Markus Ulbricht (IHP, D), 4th Workshop on RISC-V Activities, Online, 02.12.2021

Keynote: Towards Trustworthy RISC-V Processors for Safety-critical Applications, Eyck Jentzsch (MINRES Technologies, D), 4th Workshop on RISC-V Activities, Online, 02.12.2021

Deligiannis N. I., Cantoro, R., Faller T., Paxian T., Becker B., & Sonza Reorda, M.; Effective SAT-based Solutions for Generating Functional Sequences Maximizing the Sustained Switching Activity in a Pipelined Processor, In 2021 IEEE 30th Asian Test Symposium (ATS) (pp. 73-78); https://doi.org/10.1109/ATS52891.2021.00025.

Self-adaptive Single-Event Upset Resilience in
Reconfigurable Systems for Space Applications, J. Chen, M. Andjelkovic, M. Krstic, Presentation, 3rd ELICSIR Training School, University of Granada, https://elicsir-project.eu/index.php

Faller, Tobias, et al. "Towards SAT-Based SBST Generation for RISC-V Cores" In 2021 IEEE 22nd Latin American Test Symposium (LATS). IEEE, 2021; https://doi.org/10.1109/LATS53581.2021.9651819.

L. Lu, J. Chen, A. Breitenreiter, O. Schrape, M. Ulbricht and M. Krstic, Machine Learning Approach for Accelerating Simulation-based Fault Injection, 2021 IEEE Nordic Circuits and Systems Conference (NorCAS), 2021, pp. 1-6, https://doi.org/10.1109/NorCAS53631.2021.9599646.

Automated HW/SW Co-design for Edge AI: State, Challenges and Steps Ahead, Oliver Bringmann1, Wolfgang Ecker2, Ingo Feldner3, Adrian Frischknecht1,Christoph Gerum1,Timo Hämäläinen4, Muhammad Abdullah Hanif5, Michael J. Klaiber3, Daniel Müller-Gritschneder6, Paul Palomero Bernardo1,Sebastian Prebeck2, Muhammad Shafique7; 1 University of Tübingen, 2 Infineon Technologies AG, 3 Bosch Corporate Research, 4 Tampere University, 5 Technische Universität Wien, 6 Technical University of Munich, 7 New York University Abu Dhabi, Special Session, ESWEEK 2021, Virtual Conference, October 10 – 15, 2021

R. Sarić et al., "Classification of Space Particle Events using Supervised Machine Learning Algorithms," 2021 IEEE 8th International Conference on Data Science and Advanced Analytics (DSAA), 2021, pp. 1-10, https://doi.org/10.1109/DSAA53316.2021.9564114.

Metamorphic Testing for Processor Verification: A RISC-V Case Study at the Instruction Level, Frank Riese1 Vladimir Herdt1;2 Daniel Große3 Rolf Drechsler1;2 1Cyber-Physical Systems, DFKI GmbH, 28359 Bremen, Germany 2Institute of Computer Science, University of Bremen, Germany 3Institute for Complex Systems, Johannes Kepler University Linz, Austria, VLSI SoC 2021, virtuell

Hardware-aware Edge AI using the parameterizable ML accelerator UltraTrail, Paul Palomero Bernardo, tinyML Talks, September 23, 2021; https://www.youtube.com/watch?v=a7X1qx8gTuA

O. Schrape, M. Andjelković, A. Breitenreiter, S. Zeidler, A. Balashov and M. Krstić, "Design and Evaluation of Radiation-Hardened Standard Cell Flip-Flops," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 68, no. 11, pp. 4796-4809, Nov. 2021, https://doi.org/10.1109/TCSI.2021.3109080.

In-Vivo Stack Overflow Detection and Stack Size Estimation for Low-End Multithreaded Operating Systems using Virtual Prototypes, Sören Tempel, Vladimir Herdt, Rolf Drechsler. FDL 2021, Antibes, France.

RISC-V AMS VP: An Open Source Evaluation Platform for Cyber-Physical Systems, Sallar Ahmadi-Pour, Vladimir Herdt, Rolf Drechsler. FDL 2021, Antibes, France.

An Open-Source Framework for FPGA Emulation of Analog/Mixed-Signal Integrated Circuit Designs. Steven Herbst1 , Gabriel Rutsch2, Wolfgang Ecker2, Mark Horowitz1 – Stanford University1, Infineon Technologies2: IEEE Trans. Comput. Aided Des. Integr. Circuits Syst. 41(7): 2223-2236 (2022); https://doi.org/10.1109/TCAD.2021.3102516

Rafael Stahl, „Utilizing Static Code Generation in TinyML“, in “tinyML EMEA Technical Forum”, June 2021, https://www.tinyml.org/event/emea-2021/ [11], Recording available: https://youtu.be/ix_J5E_SIog

Exploring Static Code Generation and SIMD-Acceleration for Machine Learning on RISC-V, Rafael Stahl, Technical University of Munich, RISC-V Forum on "Developer Tools & Tool Chains", 2.6.2021; https://riscvforumdttc2021.sched.com/event/jGkT [12], Recording available: https://youtu.be/NLGAjdVIzkk

MicroRV32: An Open Source RISC-V Cross-Level Platform for Education and Research, Sallar Ahmadi-Pour, Vladimir Herdt, Rolf Drechsler. DESTION 2021, virtuell; https://cps-vo.org/group/DESTION2021/program; [13] https://agra.informatik.uni-bremen.de/doc/work/destion2021-final45.pdf

Krishnamurthy, Pradeep, & Poppen, Frank. (2021, May 17). Implementing VexRiscv Based Murax SoC on Arty A7 Artix-7 PCB from Digilent and Enabling JTAG Connection through Xilinx's BSCANE2 Debug IP. Zenodo. http://doi.org/10.5281/zenodo.4767195

Towards RISC-V CSR Compliance Testing, Niklas Bruns, Vladimir Herdt, Daniel Große, Senior Member, University of Bremen, IEEE and Rolf Drechsler, Fellow, IEEE; IEEE EMBEDDED SYSTEMS LETTERS (ESL) journal, VOL. 13, NO. 1, MARCH 2021

New Techniques for the Automatic Identification of Uncontrollable Lines in a CPU Core, Nikolaos I. Deligiannis[1], Riccardo Cantoro[1], Matthias Sauer[3], Bernd Becker[2], Matteo Sonza Reorda[1], [2]Univ. of Freiburg - Freiburg, Germany, [1]Politecnico di Torino, DAUIN - Torino, Italy, [3]Advantest - Böblingen, Germany, 25-28.4.2021, IEEE VLSI Test Symposium (VTS) 2021, Virtual; https://doi.org/10.1109/VTS50974.2021.9441040

Adaptive Simulation with Virtual Prototypes in an Open-Source RISC-V Evaluation Platform, Vladimir Herdt1;2 Daniel Große2;3 Sören Tempel1 Rolf Drechsler1;2, 1Institute of Computer Science, University of Bremen, Bremen, Germany, 2Cyber-Physical Systems, DFKI GmbH, Bremen, Germany, 3Institute for Complex Systems, Johannes Kepler University Linz, Austria in Journal of Systems Architecture (JSA), Elsvier, 2021; https://doi.org/10.1016/j.sysarc.2021.102135

Scale4Edge RISC-V Computing Ecosystem: Virtual Prototyping First!, Wolfgang Ecker, Daniel Mueller-Gritschneder, Ingo Feldner, Vladimir Herdt, Eyck Jentzsch, Christian Mayr, Oliver Bringmann, Johannes Partzsch, Paul Palomero Bernardo, Embedded IoT World 2021, March 30-31 2021

FZI plant ein Arbeitsergebnis aus Scale4Edge auf dem MBMV-Workshop im Rahmen einer live Demonstration, am 19.03.2021, zu präsentieren. Für die Veröffentlichung und zur besseren Einsichtnahme findet sich das Werkzeug auf GitHub: https://github.com/fzi-forschungszentrum-informatik/chips-core [14]. Hierbei handelt es sich um die CHIPS (Chisel Hardware Property Specification) Sprache sowie unterstützendes Tooling.

CHIPS: A Property Specification and Verification Framework for RISC-V based System-on-Chip (SoC) Designs; A. Paule, O. Bringmann, MBMV 2021 Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen

Constrained Random Verification for RISC-V: Overview, Evaluation and Discussion, Sallar Ahmadi-Pour1, Vladimir Herdt1;2, Rolf Drechsler1;2, 1Institute of Computer Science, University of Bremen, Germany, 2Cyber-Physical Systems, DFKI GmbH, Bremen, Germany, MBMV, Virtuell, 18.-19.3.2021.

Register and Instruction Coverage Analysis for Different RISC-V ISA Modules, Peer Adelt, Bastian Koppelmann, Wolfgang Müller, Christoph Scheytt, Heinz Nixdorf Institut/Universität Paderborn, Paderborn, Germany, MBMV, Virtuell, 18.-19.3.2021.

On Self-Verifying DSL Generation for Embedded Systems Automation, Zhao Han1,2, Shahzaib Qazi2, Michael Werner1,2, Keerthikumara Devarajegowda1,3, Wolfgang Ecker1,2, Infineon Technologies AG1 - Technical University Munich2 - Technical University Kaiserslautern3, MBMV, Virtuell, 18.-19.3.2021.

Extending Verilator to enable Fault simulation, Endri Kaja[1,2], Nicolas Ojeda Leon[1,4], Michael Werner[1,3], Bogdan Andrei-Tabacaru[1], Keerthikumara Devarajegowda[1], Wolfgang Ecker[1,3], [1]Infineon Technologies AG, Germany, [2]Technische Universität Kaiserslautern, Germany, [3]Technische Universität München, Germany, [4]Darmstadt University of Applied Sciences, Germany, MBMV, Virtuell, 18.-19.3.2021.

MicroRV32: A SpinalHDL based RISC-V Implementation for FPGAs, Sallar Ahmadi-Pour, Vladimir Herdt, Rolf Drechsler, University Booth, DATE 2021, virtuell.

An Effective Methodology for Integrating Concolic Testing with SystemC-based Virtual Prototypes, Sören Tempel1 Vladimir Herdt1;2 Rolf Drechsler1;2, 1Institute of Computer Science, University of Bremen, Bremen, Germany, 2Cyber-Physical Systems, DFKI GmbH, Bremen, Germany, DATE 2021

Vortrag: Wolfgang Ecker European collaboration: Scale4Edge project introduction”, SOC HUB LAUNCH – BOOST COMPETITIVENESS THROUGH

SYSTEM-ON-CHIP at Tampere. Smart City Week, Online, 27.01.2021, https://smarttampere.fi/en/home/

Panel Diskussion: Wolfgang Ecker European collaboration: Scale4Edge project introduction", SOC HUB LAUNCH – BOOST COMPETITIVENESS THROUGH SYSTEM-ON-CHIP at Tampere. Smart City Week, Online, 27.01.2021, https://smarttampere.fi/en/home/

Vladimir Herdt, Sören Tempel, Daniel Große, and Rolf Drechsler; Mutation-based Compliance Testing for RISC-V; In 26th Asia and South Pacific Design Automation Conference (ASPDAC '21), January 18–21, 2021, Tokyo, Japan. ACM, New York, NY, USA, 6 pages. https://doi.org/10.1145/3394885.3431584

RISC-V Summit 2020 with "Scale4Edge project introduction" by Wolfgang Ecker, Lead Principle Engineer, Infineon Technologies, Virtual Event, Tuesday, 8 December 2020 12:00pm - 12:20pm - PST (Pacific Standard Time, GMT-8); https://tmt.knect365.com/risc-v-summit/

Vortrag auf der Onespin User-Konferenz OSMOSIS 2020: W. Kunz: "Hardware Security Verification using Unique Program Execution Checking", 1.-2.12.2020, (virtuell).

W. Kunz, M. Fadiheh: "A Formal RTL Verification Approach for Detecting Transient Execution Side Channels in Processors", Intel – IPAS Tech Sharing Forum, Dezember, 2020

W. Ecker: Vorstellung von Scale4Edge von auf der EFECS 2020, 25.-26.11.2020

V. Herdt, D. Große, S. Tempel and R. Drechsler, "Adaptive Simulation with Virtual Prototypes for RISC-V: Switching Between Fast and Accurate at Runtime," 2020 IEEE 38th International Conference on Computer Design (ICCD), Hartford, CT, USA, 2020, pp. 312-315, https://doi.org/10.1109/ICCD50377.2020.00059.

Herdt, V., Große, D., Drechsler, R. (2020). RVX - A Tool for Concolic Testing of Embedded Binaries Targeting RISC-V Platforms. In: Hung, D.V., Sokolsky, O. (eds) Automated Technology for Verification and Analysis. ATVA 2020. Lecture Notes in Computer Science(), vol 12302. Springer, Cham. https://doi.org/10.1007/978-3-030-59152-6_31

Security Issues in Hardware/Firmware interaction – Can a formal analysis of (just) the hardware help?, Johannes Müller (Technical University of Kaiserslautern, D), Workshop on RISC-V Activities 2020, 8.10.2020, Virtuell

A Configurable Virtual Prototyping Environment for Different RISC-V ISA Subsets, Peer Adelt (University of Paderborn, D), Workshop on RISC-V Activities 2020, 8.10.2020, Virtuell

Efficient RISC-V Processor Verification via Cross-Level Testing, Vladimir Herdt (University of Bremen / DFKI, D), Eyck Jentzsch (MINRES Technologies, D), Daniel Große (Johannes Kepler University Linz, AT), Rolf Drechsler (University of Bremen / DFKI, D), Workshop on RISC-V Activities 2020, 8.10.2020, Virtuell

A Compiler Comparison in the RISC-V Ecosystem, Mehrdad Poorhosseini, Kim Grüttner, Wolfgang Nebel (OFFIS, D), Workshop on RISC-V Activities 2020, 8.10.2020, Virtuell

Energy Efficient RISC-V Implementations in 22 nm, Heiner Bauer (Technical University of Dresden, D), Workshop on RISC-V Activities 2020, 8.10.2020, Virtuell

A RISC-V based Edge Computing Platform with Interchangeable Cores Using 22FDX, Paul Palomero Bernardo, Adrian Frischknecht, Dustin Peterson, University of Tuebingen, D, Workshop on RISC-V Activities 2020, 8.10.2020, Virtuell

Keynote: RISC-V Scale4Edge Ecosystem - Motivation and Objectives, Wolfgang Ecker (Infineon, D), Workshop on RISC-V Activities 2020, 8.10.2020, Virtuell

UltraTrail: A Configurable Ultralow-Power TC-ResNet AI Accelerator for Efficient Keyword Spotting by Paul Palomero Bernardo, Christoph Gerum, Adrian Frischknecht, Konstantin Lübeck, and Oliver Bringmann, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 39, Issue: 11, Nov. 2020, https://doi.org/10.1109/TCAD.2020.3012320.

Von TUK wurden vier Vortragsbeiträge zum Intel internen SCAP Workshop 2020 (virtuell) eingeladen und geleistet, 28.9.-1.10.2020.

Pressemitteilung IFX, am 24. September 2020 „Projekt Scale4Edge startet im Rahmen der Leitinitiative „Vertrauenswürdige Elektronik" des Bundesforschungsministeriums - Skalierbares Ökosystem für Spezialprozessoren für das Internet der Dinge wird angestrebt" (https://www.infineon.com/cms/de/about-infineon/press/press-releases/2020... [15])

W. Ecker: ZuSE Workshop am 22.9.2020

Best Paper Award: "Efficient Cross-Level Testing for Processor Verification: A RISC-V Case-Study", Vladimir Herdt, Daniel Große, Universität Bremen, DE, Eyck Jentzsch, MINRES Technologies GmbH, DE, Rolf Drechsler, Universität Bremen, DE, FDL 2020, September 2020

W. Ecker: Silicon Saxony: Vortrag am 11.9.2020

Vladimir Herdt, Daniel Große, Jonas Wloka, Tim Güneysu, and Rolf Drechsler. 2020. Verification of Embedded Binaries using Coverage-guided Fuzzing with SystemC-based Virtual Prototypes. In Proceedings of the 2020 on Great Lakes Symposium on VLSI (GLSVLSI '20). Association for Computing Machinery, New York, NY, USA, 101–106. https://doi.org/10.1145/3386263.3406899

Pressemitteilung OSS mit TUK, RB und MNRS, im September 2020

Pressemeldung der TU Kaiserslautern am 6.7.2020

W. Ecker: Pressekonferenz „Vertrauenswürdige Elektronik“ am 9.6.2020

HNI Newsletter Ausgabe 01 2020 der Universität Paderborn „Neues Verbundprojekt Scale4Edge“. S.8: https://www.hni.uni-paderborn.de/fileadmin/Publikationen/hni_aktuell/hni_aktuell_1_2020.pdf

Success Story: Software-Driven CPU Implementation (EKUT, MNRS, RB, Siemens, TUDA, UB, UPB), https://www.edacentrum.de/scale4edge/system/files/ct_project_news/scale4edge-success-story-audio-event-detection.pdf

muRISCV-NN Präsentation in RISC-V SIG für Graphics&ML

Das CHIPS-Framework ist eine in Scala eingebettete domänenspezifische Sprache (DSL), die die Spezifikation von leichtgewichtigen Verifikationseigenschaften auf verschiedenen Abstraktionsebenen unter Verwendung des assertion-basierten Verifikationsparadigmas ermöglicht; Open Source; https://github.com/fzi-forschungszentrum-informatik/chips-core

Rust-Bibliothek, welche eine FIRRTL-AST-Darstellung und zugehörige Managementschnittstellen, einschließlich eines Parsers und Formatierers, bereitgestellt; Open Source; https://github.com/fzi-forschungszentrum-informatik/firrtl-ast

Erweiterung des Rocket Chip Generator zur Bereitstellung von Informationen zum Register-Mapping. Diese Erweiterung ist zur Nutzung der HW/SW-Co-Verifikation notwendig. Im Rahmen der Erweiterung wurden Änderungen zur Vereinfachung des Wechsels auf Scala3 eingepflegt; Open Source; https://github.com/chipsalliance/rocket-chip

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**Source URL:** https://project.edacentrum.de/scale4edge/en/publications

**Links:**
[1] https://github.com/riscv-non-isa/riscv-trace-spec/
[2] https://doi.org/10.1109/TCAD.2024.3445810;
[3] https://dx.doi.org/10.1561/3500000003;
[4] https://www.asplos-conference.org/asplos2024/
[5] https://date24.date-conference.com/programme
[6] https://edas.info/p29519#S1569607348;
[7] https://www.intel.com/content/www/us/en/security/security-practices/security-research/hardware-security-academic-award.html
[8] https://doi.org/10.1109/DAC18074.2021.9586248;
[9] https://doi.org/10.1007/978-3-031-15074-6_16
[10] https://doi.org/10.1007/s11432-020-3308-4
[11] https://www.tinyml.org/event/emea-2021/
[12] https://riscvforumdttc2021.sched.com/event/jGkT
[13] https://cps-vo.org/group/DESTION2021/program;
[14] https://github.com/fzi-forschungszentrum-informatik/chips-core
[15] https://www.infineon.com/cms/de/about-infineon/press/press-releases/2020/INFXX202009-090.html