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Scale4Edge @ 2022 IEEE 35th International System-on-Chip Conference (SOCC)

2022/08/19

Monday, September 5, 2022 14:05 - 15:25 (Europe/London)

Industrial Sesson: RISC-V: Evolution, Innovation and Research Challenges of Open-ISA

Room: Britannic Suite

Abstract

Standards are known to slow down research and innovation in their area. Therefore, one might fear that the RISC-V ISA, as a standard, slows down processor and ISA development.

Interestingly though, the opposite can be observed. Pushed by politicians worldwide, many research programs around RISC-V have been defined and undertaken, and more are in preparation. Further, Universities make faster progress since they can focus on dedicated research aspects since RISC-V infrastructure and high-quality reference implementations are freely available in open source. Also freely available applications and reference implementations help to validate and compare research results with existing solutions.

In this session, leading researchers and engineers from universities and industry report on their recent research and development results around RISC-V, their challenges in bringing RISC-V to life, and how RISC-V fosters their work.

Talks

- 1. "Monte Cimone: An Open RISC-V Cluster as a Research Platform for the Codesign of future RISC-V-based High Performance Computers" by Andrea Bartolini, Emanuele Parisi, Federico Ficarelli, Francesco Beneventi, Francesco Barchi, Daniele Gregori, Fabrizio Magugliani, Marco Cicala, Cosimo Gianfreda, Daniele Cesarini, Andrea Acquaviva, and Luca Benini from Universita' di Bologna, E4 Engineering, CINECA, ETHZ
- 2. "Focus: RISC-V in Innovation How to bring research to application" by Ari Kulmala, Timo Hämäläinen from SoC Hub Team at Tampere University, Finland
- 3. "An Industrial Perspective on RISC-V Innovation" by Keerthikumara Devarajegowda, Sebastian Prebeck, Endri Kaja, Nicolas Gerlin, Sven Wenzeck, Daniela Sanchez Lopera, Wolfgang Ecker from Infineon Technologies

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