Veröffentlichungen

2025/11/26

230 publications worldwide (including 133 papers, 45 presentations, 22 contributions to journals, 5 demonstrators, 4 keynotes, 2 invited talks, 1 contribution to a book, 1 white paper, 1 patent) in 136 conferences, workshops and journals
Details: https://scale4edge.edacentrum.de/en/publications [1]

Highlights:

1 Patent von UPB: “Enhanced PLL Circuit” (https://patentscope.wipo.int/search/en/detail.jsf?docId=WO2023099639 [2])

5 Best Paper | Keynote Awards (MECO 2025, FDL 2020, DAC 2022 und DATE 2023)

BEST Keynote Speech Award: Prof. Dr. Wolfgang Ecker: Infineon Technologies AG and Technical University of Munich "How to circumvent RISC-V Dead End“, MECO 2025

BEST Female Scientist Award: Natalie Simson, et. al.: Infineon Technologies AG and Technical University of Munich "Moving from RTL- to Handshake-based IP-Design: A RISC-V Case Study“, MECO 2025

HIPEAC-Award (DAC 2022)

Intel Hardware Security Academic Award 2022 - Winner First place

IEEE Top Pick in Security von RPTU „An Exhaustive Approach to Detecting Transient Execution Side Channels in RTL Designs of Processors“ in IEEE Trans. on Computers

Book „QED and Symbolic QED: Dramatic Improvements in Pre-Silicon Verification and Post-Silicon Validation” by “now publishers” with contributions from Siemens EDA, Infineon and RPTU

acatech Study „Edge AI: KI nahe am Endgerät. Technologie für mehr Datenschutz, Energieeffizienz und Anwendungen in Echtzeit“ (in German only) by Infineon and TUM with Bosch and University of Tübingen

„Embench™ IOT 2.0 and DSP 1.0: Modern Embedded Computing Benchmarks“ David Patterson et. al. with Co-Autors from Hochschule München University of Applied Sciences in IEEE Computer Volume: 58, Issue: 5, May 2025

Smart Video Capsule Endoscopy: Raw Image-Based Localization for Enhanced GI Tract Investigation, Oliver Bause*, Julia Werner*, Paul Palomero Bernardo, and Oliver Bringmann (*Equal Contribution), 32nd International Conference on Neural Information Processing (ICONIP), 2025;

Automatic Cell-Aware Software-Based Self-Test Generation for a RISC-V Core Local Interrupt Controller, Tobias Faller, Bernd Becker, IEEE ATS 2025, Tokyo / Japan

Comparing Methods for the Cross-Level Verification of SystemC Peripherals with Symbolic Execution; Karl Aaron Rudkowski (1), Sallar Ahmadi-Pour (1), Rolf Drechsler (1,2), (1) Institute of Computer Science, University of Bremen, Germany, (2) Cyber-Physical Systems, DFKI GmbH, Bremen, Germany; IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems; December 2025.

A 50 Gbps Reference-Less NRZ Full-Rate Bang-Bang CDR with Automatic Frequency Acquisition in 130nm SiGe:C BiCMOS Technology, M. Iftekhar, B. Sadiye, W. Mueller and J. C. Scheytt, 2025 IEEE Nordic Circuits and Systems Conference (NorCAS), Riga, Latvia, 2025, pp. 1-7, doi: 10.1109/NorCAS66540.2025.11231203.

60-Gb/s 1:4 Demultiplexer in 22-nm FD-SOI Technology Using TSPC Logic: A Circuit-to-System-Level Analysis and Design, B. Sadiye, M. Iftekhar, W. Mueller and J. C. Scheytt, in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, doi: 10.1109/TVLSI.2025.3625787.

A Quantitative Guide to Navigate Speed/Accuracy Tradeoffs in System Level Design of RISC-V Processor Grids, L. Luchterhandt, V. Govindasamy, Y. Wang, C. Scheytt, W. Mueller and R. Dömer, 2025 Forum on Specification & Design Languages (FDL), St. Goar, Germany, 2025, pp. 1-9, doi: 10.1109/FDL68117.2025.11165408.

Accelerate SEU Simulation-based Fault Injection with Spatio-Temporal Graph Convolutional Networks; L. Lu; J.-C. Chen, A. Balakrishnan, M. Ulbricht, M. Krstic; IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems;

Agile Methodologies for the Development of Radiation-Hardened Integrated Circuits; J.-C. Chen; L. Lu, A. Veronsi, M. Andjelkovic, M. Krstic; The European Physical Journal Special Topics;

Dynamic Fault Mitigation for Space Radiation using Fault Injection and Machine Learning; J.-C. Chen; L. Lu, M. Andjelkovic, F. Vargas, M. Krstic; Journal of Electronic Testing;

Self-Adaptive Fault Resilience for Processing Systems in Space Applications; J.-C. Chen; M. Andjelkovic, L. Lu, M. Ulbricht, M. Krstic; IEEE Access;

B. M. Damian-Kosterhon, F. Meisel and A. Koch, SCAL: An Open-Source Scalable Core Adaptation Layer for Interfacing RISC-V ISA Extensions, 2025 IEEE 36th International Conference on Application-specific Systems, Architectures and Processors (ASAP), Vancouver, BC, Canada, 2025, pp. 73-80, doi: 10.1109/ASAP65064.2025.00020. keywords: {Microarchitecture;Instruction sets;Semantics;Pipelines;Ecosystems;Systems architecture;Hazards;Resource management;SCAIE-V;ISAX;Portability;RISC-V},

Edge AI: KI nahe am Endgerät - Technologie für mehr Datenschutz, Energieeffizienz und Anwendungen in Echtzeit; Ecker, W., Houdeau, D. et al.; 2025;

Moving from RTL- to Handshake-based IP-Design: A RISC-V Case Study; Natalie Simson, Paritosh Kumar Sinha, Wolfgang Ecker. Best Paper Awarded

How to Acoid RISCV Dead End ; Wolfgang Ecker,

Evaluating the Vulnerabilities of TETRISC SoC Under Laser Fault Injection; J.-C. Chen; D. Petryk, M. Ulbricht, M. Krstic; Proc. 1st Workshop on Reliable and Secure RISC-V Architectures (RESCUER 2025);

Design to Deploy: Platform–Aware RTL Code Generation for Optimized Performance, Testability, and Safety; Mohamed Badawy, Nicolas Gerlin, Paritosh Kumar Sinha, Endri Kaja, Jad Al Halabi, Stephanie Ecker, Natalie Simson, Wolfgang Ecker; ETS 2025, May 26 - 30, 2025 Tallinn, ESTONIA

Prototyping custom RISC-V instructions with Seal5 and CoreDSL, Jan Schlamelcher, Thomas Goodfellow, Bewoayia Kebianyor, Gregor Nitsche, Philipp Van Kempen (TUM), Kim Grüttner RISC-V Summit Europe, 2025-05-12 - 2025-05-15, Paris, Frankreich.

Benchmarking TinyML CNN Kernels on RVV 1.0 Hardware: GCC 14 vs. LLVM 19, Philipp van Kempen, Benedikt Witteler, Ulf Schlichtmann (TUM), Daniel Mueller-Gritschneder (TUW), Extended Abstract, RISC-V Summit Europe 2025, 12.-15.5.2025, Paris

Benchmarking TinyML CNN Kernels on RVV 1.0 Hardware: GCC 14 vs. LLVM 19, Philipp van Kempen, Benedikt Witteler, Ulf Schlichtmann (TUM), Daniel Mueller-Gritschneder (TUW), Poster, RISC-V Summit Europe 2025, 12.-15.5.2025, Paris

Implementation of Dynamic SISD-SIMD Integer Dividers; Gianluca Radi, Ares Tahiraga, Robert Kunzelmann, Ties Jan Henderikus Kluter, Wolfgang Ecker

Tracing-Bibliothek nach der ETrace-Spezifikation (https://github.com/riscv-non-isa/riscv-trace-spec/ [3]), FZI

LLM-assisted Methodology for Embedded Software Performance Estimation on RISC-V, Weiyan Zhang <weiyan@uni-bremen [dot] de> (1), Muhammad Hassan (1,2), and Rolf Drechsler (1,2), (1) Institute of Computer Science, University of Bremen, Germany, (2) Cyber-Physical Systems, DFKI GmbH, Bremen, Germany, RISC-V Summit Europe 2025, 12.05.2025 - 15.05.2025, Paris, FR.

CrosSym: Cross-Level Verification of SystemC Peripherals using Symbolic Execution, Karl Aaron Rudkowski <karlaaron@uni-bremen [dot] de> (1), Sallar Ahmadi-Pour (1), and Rolf Drechsler (1,2), (1) Institute of Computer Science, University of Bremen, Germany, (2) Cyber-Physical Systems, DFKI GmbH, Bremen, Germany, DDECS 2025, 05.05.2025 - 07.05.2025, Lyon, FR.

LLM-assisted Performance Estimation of Embedded Software on RISC-V Processors, Weiyan Zhang <weiyan@uni-bremen [dot] de> (1), Muhammad Hassan (1,2), and Rolf Drechsler (1,2), (1) Institute of Computer Science, University of Bremen, Germany, (2) Cyber-Physical Systems, DFKI GmbH, Bremen, Germany, DDECS 2025, 05.05.2025 - 07.05.2025, Lyon, FR.

On April 4 2025, EPoSS and INSIDE industry associations hosted a webinar outlining Europe’s strategic direction in Edge AI, a domain at the forefront of AI innovation.

These are the key takeaways:

Cooperation before competition: European tech leaders emphasized the need for a united front to build competitive ecosystems.
Edge AI is accelerating: From LLMs to digital twins and frugal AI, innovation is rapidly reshaping the edge computing stack.
Cross-layer optimization is crucial: True impact requires co-design across chips, software, and applications.

Europe must act now: Limited access to advanced nodes and reliance on non-EU infrastructure highlight the urgency for investment and collaboration.
A call to action: The Edge AI Working Group is advocating for a European roadmap, open ecosystems, and robust training infrastructure.
Short reports on all parts of the workshop are now available for download. Our special thanks go all contributors and presenters:

Inessa Seifert, VDI/VDE-IT
Paolo Azzoni, INSIDE
Danilo Pau, STMicroelectronics
Anders Lindgren, RISE
Alain Pagani, German Research Center for Artificial Intelligence (DFKI)
Hans-Jörg Vögel, BMW
Lior Klein, MultiSpin.AI
Davis Sawyer, NXP
Wolfgang Ecker, Infineon
Downloads: https://www.smart-systems-integration.org/publication/future-edge-ai-notes-workshop

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Case Study on Combining Open-Source Tool Flows for Grids of Processing Cells, L. Luchterhandt, V. Govindasamy, Y. Wang, C. Scheytt, W. Mueller and R. Dömer, OSSMPIC Workshop, Lyon, March 2025.

Paul Palomero Bernardo, Patrick Schmid, Christoph Gerum, and Oliver Bringmann. 2025. Compiler-aware AI Hardware Design for Edge Devices. In The 8th International Workshop on Edge Systems, Analytics and Networking (EdgeSys '25), March 30-April 3, 2025, Rotterdam, Netherlands. ACM, New York, NY, USA, 6 pages. https://doi.org/10.1145/3721888.3722095

A Hardware-assisted Approach for Non-invasive and Fine-grained Memory Power Management in MCUs, Michael Kuhn, Patrick Schmid and Oliver Bringmann, Embedded Systems, University of Tübingen, Germany, DATE 2025, 31.3-2.4.2025, Lyon, France.

Towards Non-Intrusive SystemC Checkpointing for Digital Virtual Prototypes, Deepak Ravibabu (1), Muhammad Hassan <hassan@uni-bremen [dot] de> (1,3), Thilo Vörtler (2), Karsten Einwich (2), Rolf Drechsler (1,3), and Daniel Große (1,4); (1) Cyber-Physical Systems, DFKI GmbH, 28359 Bremen, Germany, (2) COSEDA Technologies GmbH, 01099 Dresden, Germany, (3) Institute of Computer Science, Bremen University, 28359 Bremen, Germany, (4) Institute for Complex Systems, Johannes Kepler University, 4040 Linz, Austria, MBMV-Workshop, 11.03.2025, Rostock, DE.

Symbolic Execution of Unmodified SystemC Peripherals, Karl Aaron Rudkowski <karlaaron@uni-bremen [dot] de> (1), Sallar Ahmadi-Pour (1), and Rolf Drechsler (1,2), (1) Institute of Computer Science, University of Bremen, Germany, (2) Cyber-Physical Systems, DFKI GmbH, Bremen, Germany, MBMV-Workshop, 11.03.2025, Rostock, DE.

Improving Design Generation by Interface Configuration Propagation Natalie Simson, Infineon Technologies AG and Technical University of Munich, DE, <natalie [dot] simson@infineon [dot] com>, Paritosh Kumar Sinha, Infineon Technologies AG, DE, Wolfgang Ecker, Infineon Technologies AG and Technical University of Munich, DE, MBMV-Workshop, 11.03.2025, Rostock, DE.

Platform-Aware RTL Generation: Bridging the Gap between Design and Implementation Mohamed Badawy, Infineon Technologies AG, DE <mohamed [dot] badawy@infineon [dot] com>, Nicolas Gerlin, Paritosh Kumar Sinha, Endri Kaja, Jad Al Halabi, Stephanie Ecker, Natalie Simson, Wolfgang Ecker, Infineon Technologies AG and Technical University of Munich, DE, MBMV-Workshop, 11.3.2025, Rostock, DE.

Parameterized Construction and Constraint-Driven Validation of Formal Hardware Specifications for Efficient Code Generation, Robert Kunzelmann, Infineon Technologies AG and Technical University of Munich, DE <robertniklas [dot] kunzelmann@infineon [dot] com>, Maximilian Berger, Infineon Technologies AG, DE and Technical University of Munich, DE, Wolfgang Ecker, Infineon Technologies AG and Technical University of Munich, DE, MBMV-Workshop, 11.3.2025, Rostock, DE.

Verilator and FireSim RTL Simulations on a HPC Cluster: A Comparative Case Study, Kai Hannemann, Universität Paderborn, DE <kaiha@hni [dot] uni-paderborn [dot] de>, Hüseyin Berke Bütün, Wolfgang Mueller, Christoph J. Scheytt, MBMV-Workshop, 11.3.2025, Rostock, DE.

N-Modular Redundancy Controller Generator for Adaptive Fault Tolerance Systems; J.-C. Chen; M. Ulbricht, M. Krstic; Proc. 37. ITG/GMM/GI-Workshop Testmethoden und Zuverlässigkeit von Schaltungen und Systemen (TuZ 2025), (2025);

Towards Adaptive RISC-V based Systems for Non-Terrestrial Sub-THz Communication; H. Borchert; M. Ulbricht, M. Andjelkovic, D. Göhringer, M. Krstic; Proc. International Conference on Mobile and Miniaturized Terahertz Systems (ICMMTS 2025), (2025);

Execute Your Darlings: Dynamic Execution of High-Level Formal Specifications for Validation and Early Prototyping, Robert Kunzelmann, Infineon Technologies AG and Technical University of Munich, DE, Zeyad Tahoun, Infineon Technologies AG, DE and Politecnico di Torino, IT, Wolfgang Ecker, Infineon Technologies AG and Technical University of Munich, DE, RAPIDO-Workshop @ HiPEAC, 21.1.2025, Barcelona, ES.

Design and Analysis of an Adaptive Radiation Resilient RRAM Subsystem for Processing Systems in Satellites; D. Reiser; J.-C. Chen, J. Knödtel, M.

Krstic, M. Reichenbach; Design Automation for Embedded Systems;

P. Schmid, P. Palomero Bernardo, C. Gerum and O. Bringmann, GOURD: Tensorizing Streaming Applications to Generate Multi-Instance Compute Platforms, in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 43, no. 11, pp. 4166-4177, 6.11.2024, https://doi.org/10.1109/TCAD.2024.3445810; [4] https://ieeexplore.ieee.org/abstract/document/10745814.

VeriCHERI: Exhaustive Formal Security Verification of CHERI at the RTL, Anna Lena Duque Antón∗, Johannes Müller∗, Philipp Schmitz, Tobias Jauch, Alex Wezel, Lucas Deutschmann, Mohammad R. Fadiheh, Dominik Stoffel, Wolfgang Kunz, RPTU Kaiserslautern-Landau, ∗Both authors contributed equally to this research, ICCAD 2024, October 27–31, 2024, New York, NY, USA

Keerthikumara Devarajegowda, Florian Lonsing, Mohammad R. Fadiheh, Saranyu Chattopadhyay, David Lin, Srinivas Shashank Nuthakki, Eshan Singh, Clark Barrett, Wolfgang Ecker, Wolfgang Kunz, Yanjing Li, Dominik Stoffel and Subhasish Mitra (2024), QED and Symbolic QED: Dramatic Improvements in Pre-Silicon Verification and Post-Silicon Validation, Foundations and Trends® in Integrated Circuits and Systems: Vol. 3: No. 2–3, pp 51-217. https://dx.doi.org/10.1561/3500000003; [5] 23.20.2024

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SIZALIZER: Multilevel Analysis Framework for Object Size Optimization, Andreas Hager-Clukas, Jonathan Schröter, and Stefan Wallentowitz, Hochschule München University of Applied Sciences, International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation (SAMOS), June 29 - July 4, 2024.

MCU-Wide Timing Side Channels and Their Detection, Johannes Müller1, Anna Lena Duque Antón1, Lucas Deutschmann1, Dino Mehmedagić1, Cristiano Rodrigues2, Daniel Oliveira2, Keerthikumara Devarajegowda3, Mohammad Rahmani Fadiheh4, Sandro Pinto2, Dominik Stoffel1, and Wolfgang Kunz1 1RPTU Kaiserslautern-Landau, 2Universidade do Minho, 3Siemens EDA, 4Stanford University, DAC 2024

Unique Program Execution Checking: Formal Security Guarantees for RISC-V Systems, Alex Wezel, Lucas Deutschmann, Tobias Jauch, Dino Mehmedagić, Johannes Müller, Mohamed Ali, Anna Lena Duque Antón, Philipp Schmitz, Mohammad Rahmani Fadiheh, Dominik Stoffel, Wolfgang Kunz, Übersichtsvortrag, RISC-V Summit Europe 2024, 24.-28.6.2024, München

Cross-Level Verification of Hardware Peripherals, Sallar Ahmadi-Pour1, Muhammad Hassan1,2, Rolf Drechsler1,2 *, 1Institute of Computer Science, University of Bremen, Germany, 2Cyber-Physical Systems, DFKI GmbH, Germany, RISC-V Summit Europe 2024, Munich, Germany 24-28 June 2024.

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A Universal Specification Methodology for Quality Ensured, Highly Automated Generation of Design Models; Robert Kunzelmann1, 2, Emil Baerens1, Daniel Gerl1, 2, Mayuri Bhadra1, 2, Niklas Schwarz1, and Wolfgang Ecker1, 2; 1Infineon Technologies AG, Neubiberg, Germany; 2Technical University of Munich, Munich, Germany, MBMV 2024, 14.+15.2.2024, Kaiserslautern, Germany

Extending Clang/LLVM with Custom Instructions using TableGen – An Experience Report; Jan Schlamelcher, Thomas Goodfellow, Bewoayia Kebianyor, and Kim Grüttner, German Aerospace Center - Institute of Systems Engineering for Future Mobility, MBMV 2024, 14.+15.2.2024, Kaiserslautern, Germany

A Concise, Architecture-Focused ASIP Modeling Approach for Instruction Set Simulators; Karsten Emrich, Daniel Mueller-Gritschneder, Ulf Schlichtmann, Chair of Electronic Design Automation, Technical University of Munich, MBMV 2024, 14.+15.2.2024, Kaiserslautern, Germany

Next-Gen TETRISC SoC - A Quad-Heterogeneous Design for Adaptive Fault Tolerance; J.-C. Chen; L. Lu, M. Ulbricht, M. Krstic; Proc. RISC-V Summit Europe (RISC-V 2024);

muRISCV-NN: Challenging Zve32x Autovectorization with TinyML Inference Library for RISC-V Vector Extension, Philipp van Kempen1, Jefferson Parker Jones1, Daniel Mueller-Gritschneder2, Ulf Schlichtmann1, 1Technical University of Munich, 2Vienna University of Technology, CF24-OSHW, Workshop on Open-Source Hardware, Co-located with 21th ACM International Conference on Computing Frontiers (CF’ 24) May 7 - May 9, 2024 - Ischia (NA), Italy

Longnail: High-Level Synthesis of Portable Custom Instruction Set Extensions for RISC-V Processors from Descriptions in the Open-Source CoreDSL Language, Julian Oppermann1, Brindusa Mihaela Damian-Kosterhon1, Florian Meisel1, Tammo Mürmann1, Eyck Jentzsch2, Andreas

Koch1, 1Technical University of Darmstadt, 2MINRES Technologies Munich, International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), https://www.asplos-conference.org/asplos2024/ [6], San Diego, USA — April 27- May 1, 2024

Data-Oblivious and Performant: On Designing Security-Conscious Hardware, Lucas Deutschmann∗, Yazan Kazhalawi∗, Jonathan Seckinger∗, Anna Lena Duque Antón∗, Johannes Müller∗, Mohammad Rahmani Fadiheh†, Dominik Stoffel∗, Wolfgang Kunz∗; ∗RPTU Kaiserslautern-Landau, Kaiserslautern, Germany †Stanford University, Stanford, US, LATS 2024; Maceió, BR, https://cas.polito.it/LATS2024/program

Space Radiation Flux Driven Fault Injection for Evaluating Dynamic Mitigation Strategies; J.-C. Chen; L. Lu, M. Andjelkovic, F. Vargas, M. Krstic; Proc. 25th IEEE Latin American Test Symposium (LATS 2024), (2024);

TUDD Demo: ZuSE Scale4Edge – AI Hardware Accelerator for Ultra-Low-Power Keyword Spotting, ADTC + edaWorkshop24, Dresden, 9.+11.4.2024

Ein KI-Hardware-Beschleuniger für ultra-energieeffiziente Schlüsselworterkennung wird demonstriert. Durch Optimierung der Vorverarbeitung, Ausnutzung von Sparsity in einem Beschleuniger für rekurrente neuronale Netzwerke sowie einen hierarchischen Aufwachmechanismus erreichen wir eine sehr niedrige Leistungsaufnahme bei gleichzeitig hoher Klassifikationsgüte.

IHP Demo: ZuSE Scale4Edge – Der TETRISC SoC - unser RISC-V-basiertes, fehlertolerantes Mehrkernsystem auf FPGA und gefertigt als ASIC, ADTC + edaWorkshop24, Dresden, 9.+11.4.2024

Unser Demonstrator präsentiert zwei Ausführungen des adaptiven und fehlertoleranten TETRISC SoC. Zum einen umfasst er eine prototypische Implementierung auf FPGA, mit der wir gezielt Fehler einspeisen können, um die Fehlertoleranz des Systems zu demonstrieren. Zum anderen präsentieren wir die finale Version, gefertigt in IHP 130nm Technologie. Diese zeigt die Realisierbarkeit und Funktionalität des Systems und ermöglicht Messungen zur Geschwindigkeit und Stromaufnahme.

UFR Demo: ZuSE Scale4Edge – Software-based Self-Test Generation for RISC-V, FPGA-basierter Demonstrator

Ein FPGA-basierter Demonstrator mit einem RISC-V Prozessorkern, welcher die LED-Anzeigen auf der Demoplatine steuert und periodisch einen Selbsttest ausführt. Die SBST ist für den Test der Arithmetic Logic Unit (ALU) und die Registerbank des verwendeten RISC-V Prozessorkernes ausgelegt. Über Schalter können ausgewählte Fehler in den Prozessorkern injiziert werden, welcher dann mittels des SBSTs diese detektiert, und auf den Anzeigen das Testergebnis signalisiert.

Poster: Trust & Security-Forschungen in Scale4Edge und VE-VIDES durch die Werkzeuge Questa Verify Secure und Questa Verify Trust, Jörg Bormann, Siemens EDA, ADTC + edaWorkshop24, Dresden, 9.+11.4.2024

TUDD-Poster: AI Hardware Accelerator for Ultra-Low-Power Keyword Spotting, Johannes Partzsch, TU Dresden, ADTC + edaWorkshop24, Dresden, 9.+11.4.2024

TUDD-Demo: AI Hardware Accelerator for Ultra-Low-Power Keyword Spotting, Johannes Partzsch, TU Dresden, ADTC + edaWorkshop24, Dresden, 9.+11.4.2024

Success Story: Energy-efficient Keyword-Spotting (TUDD, MNRS, SCS), https://project.edacentrum.de/scale4edge/system/files/ct_project_news/scale4edge-success-story-keyword-spotting.pdf

A Golden-Free Formal Method for Trojan Detection in Non-Interfering Accelerators, Anna Lena Duque Antón (RPTU), Johannes Müller (RPTU), Lucas Deutschmann (RPTU), Mohammad Rahmani Fadiheh (Stanford University), Dominik Stoffel (RPTU), Wolfgang Kunz (RPTU); DATE 2024

A Self-Adaptive Resilient Method for Implementing and Managing the High-Reliability Processing System; J.-C. Chen; M. Krstic; Proc. 27th Design, Automation and Test in Europe (DATE 2024);

A Scalable RISC-V Hardware Platform for Intelligent Sensor Processing; Paul Palomero Bernardo, Patrick Schmid, Oliver Bringmann, University of Tübingen, Mohammed Iftekhar, Babak Sadiye, Wolfgang Müller Paderborn University / Heinz Nixdorf Institute, Andreas Koch, Technical University of Darmstadt, Eyck Jentzsch, MINRES Technologies GmbH, Axel Sauer, Ingo Feldner, Robert Bosch GmbH, Wolfgang Ecker, Infineon Technologies AG; 25.-27.3.2024 at Design, Automation and Test in Europe (DATE) Conference 2024, Valencia, ES (https://date24.date-conference.com/programme [7]).

A Scalable Formal Verification Methodology for Data-Oblivious Hardware, Lucas Deutschmann (1), Johannes Müller (1), Mohammad R. Fadiheh (2), Dominik Stoffel (1), and Wolfgang Kunz (1); (1) University of Kaiserslautern-Landau, Kaiserslautern, Germany, (2) Stanford University, Stanford, USA, TCAD 2024; https://doi.org/10.1109/TCAD.2024.3374249

Ein Ansatz zur Optimierung konfigurierbarer fehlertoleranter Systeme; M. Ulbricht; M. Krstic; Proc. 36. ITG/GMM/GI-Workshop Testmethoden und Zuverlässigkeit von Schaltungen und Systemen (TuZ 2024), 12 (2024);

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Success Story: Multi-Compiler Support (IFX, AbsInt, DLR), https://project.edacentrum.de/scale4edge/system/files/ct_project_news/scale4edge-success-story-compilers.pdf

J. Kappes, R. Kunzelmann, K. Emrich, C. Foik, D. Mueller-Gritschneder and W. Ecker, Effective Processor Model Generation from Instruction Set Simulator to Hardware Design, 2023 IEEE Nordic Circuits and Systems Conference (NorCAS), Aalborg, Denmark, 2023, pp. 1-7, https://doi.org/10.1109/NorCAS58970.2023.10305465.

A RISC-V MCU with adaptive reverse body bias and ultra-low-power retention mode in 22 nm FD-SOI; Heiner Bauer, Marco Stolba, Stefan Scholze, Dennis Walter, Christian Mayr, Electrical and Computer Engineering Dept., TU Dresden, Germany, Alexander Oefelein, Sebastian Höppner, André Scharfe, Flo Schraut, Holger Eisenreich, Racyics GmbH, Dresden, Germany, 20th International SoC Conference (ISOCC 2023) will be held from October 25 to 28, 2023 at at the Ramada Plaza Jeju Hotel in Jeju Island, Korea, https://isocc.org.

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Minimally Invasive Generation of RISC-V Instruction Set Simulators from Formal ISA Models; Sören Tempel1 Tobias Brandt Christoph Lüth1,2 Rolf Drechsler1,2; 1Institute of Computer Science, University of Bremen, Germany; 2Cyber-Physical Systems, DFKI GmbH, Bremen, Germany; FDL 2023

Virtual Prototype driven Application Specific Hardware Optimization; Jan Zielasko1 Rolf Drechsler1,2; 1Cyber-Physical Systems, DFKI GmbH, Germany; 2Institute of Computer Science, University of Bremen, Germany; FDL 2023

Identification of ISA-Level Mutation-Classes for Qualification of RISC-V Formal Verification, Milan Funck1 Sallar Ahmadi-Pour2 Vladimir Herdt1,2 Rolf Drechsler1,2; 1Cyber-Physical Systems, DFKI GmbH, Bremen, Germany; 2Institute of Computer Science, University of Bremen, Bremen, Germany; FDL 2023

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muRISCV-NN Präsentation in RISC-V SIG für Graphics&ML

Das CHIPS-Framework ist eine in Scala eingebettete domänenspezifische Sprache (DSL), die die Spezifikation von leichtgewichtigen Verifikationseigenschaften auf verschiedenen Abstraktionsebenen unter Verwendung des assertion-basierten Verifikationsparadigmas ermöglicht; Open Source; https://github.com/fzi-forschungszentrum-informatik/chips-core

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Erweiterung des Rocket Chip Generator zur Bereitstellung von Informationen zum Register-Mapping. Diese Erweiterung ist zur Nutzung der HW/SW-Co-Verifikation notwendig. Im Rahmen der Erweiterung wurden Änderungen zur Vereinfachung des Wechsels auf Scala3 eingepflegt; Open Source; https://github.com/chipsalliance/rocket-chip

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The Scale4Edge project (project label 16ME0122K-140, 16ME0465, 16ME0900, 16ME0901) is supported by the German Federal Ministry of Research, Technology and Space (BMFTR).

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