Scale4Edge

Projekt Nachrichten

Date	Title
2023/08/09 - 14:55	Registration for Attending the RVF (RISC-V FW) - Workshop
2023/05/05 - 05:41	Success Story: The Scale4Edge Hardware Verification and Validation Ecosystem for RISC-V Platforms
2022/11/28 - 17:16	Success Story: Software-driven CPU implementation
2022/08/19 - 21:04	Scale4Edge @ 2022 IEEE 35th International System-on-Chip Conference (SOCC)
2022/06/21 - 13:32	Bringing TinyML to RISC-V With Specialized Kernels and a Static Code Generator Approach
2021/05/14 - 11:03	Exploring Static Code Generation and SIMD-Acceleration for Machine Learning on RISC-V by Rafael Stahl, Technical University of Munich @RISC-V Forum on "Developer Tools & Tool Chains" on June 2, 2021 18:05 CEST
2021/05/04 - 17:35	RISC-V Summit 2020: Tutorial with OpenHW and Silicon Labs
2021/03/16 - 16:39	Scale4Edge Partner MINRES @ Accellera's SystemC Evolution Fika
2021/03/15 - 20:31	Scale4Edge Projektpartner TU Dresden gewinnt den Pilotinnovationswettbewerb "Energieeffizientes KI-System"
2021/02/25 - 09:58	Join Scale4Edge Session on April 28, 2021 20:15 CET

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