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## edaForum02 - Program

At this web page you find the programme of the edaForum02. You may expand the programme for each session by clicking on the session title. You will find the detailed timetable, presentation titles and author names. If additional information like an abstract, curriculum vitae or (for attendees of the edaForum02 only) slides is available, a link below the presentation title is displayed.

You may [download](#) the programme as PDF file (93.51 K).

### Thursday, December 5, 2002

**09:30 - 12:30**

#### Company Presentations

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09:30 **Mentor Graphics Corp.Synthesis and Analysis of Complete Systems**, Room 1

09:30 **Cadence Design Systems, Inc. System Modelling and Physical Prototyping**, Room 2

09:30 **Verisity Design, Inc.Functional Verification -One of the Main Challenges in Todays System Designs**, Room 3

12:30 - 13:30

Lunch

**13:30 - 13:45**

#### Welcome Address

Moderator: Erich Barke (edacentrum)

**13:45 - 15:00**

#### Keynote

#### Room Atelier

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##### **The Next Big Advance in Chip-Level Design Productivity**

13:45 Richard A. Newton (U Berkeley)

[Abstract and Curriculum Vitae](#)

**15:00 - 17:15**

#### Technical Session I: Titanic Verification of Systems on Chip

#### Room A

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##### **Keynote:**

##### **The Impending Verification Revolution**

15:00 Raul Camposano (Nimbic)

[Abstract and Curriculum Vitae](#)

[Proceedings \(Access for event attendees only\)](#)

15:45

##### **Break:**

##### **Coffee Break**

16:15 **Tool-Supported Validation of Embedded Systems in Automotive Applications**

[Abstract and Curriculum Vitae](#)

##### **ROI from Nanometer IC Circuit Verification**

16:45 Sang Wang (Nassda)

[Abstract and Curriculum Vitae](#)

**15:00 - 17:15**

**Economical Session I: River of no Return EDA and Return on Investment  
Room B**

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**Keynote:**

**The Strategic Impact of the EDA Industry in the Electronics Design Chain**

15:00 Guillaume d' Eyssautier (Cadence)  
[Abstract and Curriculum Vitae](#)  
[Proceedings \(Access for event attendees only\)](#)

15:45 **Break:  
Coffee Break**

**Bright Longterm Prospects for EDA**

16:15 Peter L. Levin (TVM)  
[Abstract and Curriculum Vitae](#)

**An Analysis of the Relationship between EDA Expenditures and Competitive Positioning  
Positioning of IC Vendors**

16:45 Jordan Brysk (Ascendant Strategies Group)  
[Abstract and Curriculum Vitae](#)

17:15 - 17:45  
Break

**17:45 - 18:30  
Panel Discussion  
Room Atelier**

18:30 - 19:30  
Break

**19:30 - 23:00  
Social Event**

**Friday, December 6, 2002**

**09:00 - 11:45**

**Technical Session II: Gandhi The Dream of Analog Design Automation  
Room A**

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**Keynote:**

**Analog EDA and the Path to Practical Analog IP**

09:00 Rob A. Rutenbar (U Carnegie Mellon)  
[Abstract and Curriculum Vitae](#)  
[Proceedings \(Access for event attendees only\)](#)

**"Analog EDA: Is there Light at the End of the Tunnel ?"**

09:45 Rudolf Koch (Infineon)  
[Proceedings \(Access for event attendees only\)](#)

10:15 **Break:  
Coffee Break**

**Modeling and the Road towards True Synthesis of Analog Integrated Circuits**

10:45 Georges Gielen (U Leuven)  
[Abstract and Curriculum Vitae](#)  
[Proceedings \(Access for event attendees only\)](#)

**The Return of the Transistor**

11:15 Thomas Heydler (Barcelona)  
[Abstract and Curriculum Vitae](#)  
[Proceedings \(Access for event attendees only\)](#)

**Approaches to Formal Verification for Analog Circuits**

11:15 Lars Hedrich (U Hannover)  
[Proceedings \(Access for event attendees only\)](#)

**09:00 - 11:45**

**Economical Session II: Modern Times Benchmarking and Productivity  
Room B**

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**Keynote:**

**Methodology and Software for Maximizing Semiconductor R&D Return on Investment**

09:00 Alexander A. Silbey (Numetrics)  
[Abstract and Curriculum Vitae](#)  
[Proceedings \(Access for event attendees only\)](#)

**The Evolution of Development Processes in the Semiconductor Industry**

09:45 Fritz Kirsch (Infineon)  
[Abstract and Curriculum Vitae](#)  
[Proceedings \(Access for event attendees only\)](#)

10:15 **Break:**  
**Coffee Break**

**Investment into EDA, Its Measurable Success and its Return: The IBM Way**

10:45 Bernd-Josef Huettl (IBM)  
[Abstract and Curriculum Vitae](#)

**Full Custom Mixed-Signal-ASICs-Development: A Determinism of Art**

11:15 Peter van Staa (Robert Bosch GmbH)  
[Abstract and Curriculum Vitae](#)

11:45 - 12:15  
Break

**12:15 - 13:00**  
**Panel Discussion**  
**Room Atelier**

13:00 - 14:30  
Lunch

**14:30 - 17:00**  
**Trips & Tours**

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14:30 **Rain Forest House: In the Hannover Rain Forest House you can see, hear, smell, taste and feel the diversity of the tropical highland rain forest.**

14:30 **Sprengel-Museum: See a comprehensive Collection and diverse programme of temporary exhibitions, ranking among the major art museums of the 20th century.**

14:30 **Learning Lab Lower Saxony: L3S is a center of competence where co-operative research projects, which focus on 'collaborative learning technologies for lifelong learning', are carried out.**

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